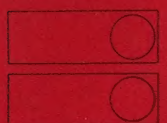
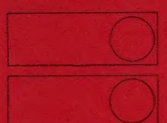




Bowmar



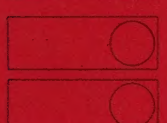
Bowmar



Bowmar



Bowmar



Bowmar



Bowmar



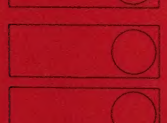
Bowmar



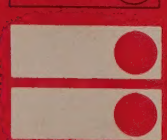
Bowmar



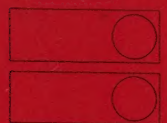
Bowmar



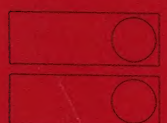
Bowmar



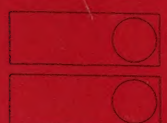
Bowmar



Bowmar



Bowmar

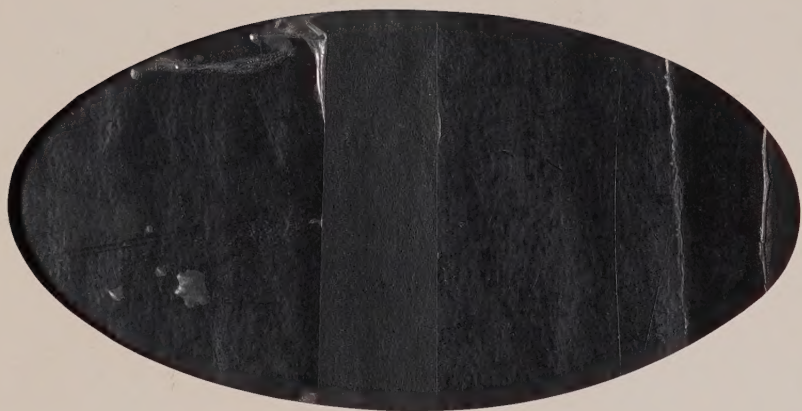


Bowmar



**Communications
Test
Equipment**

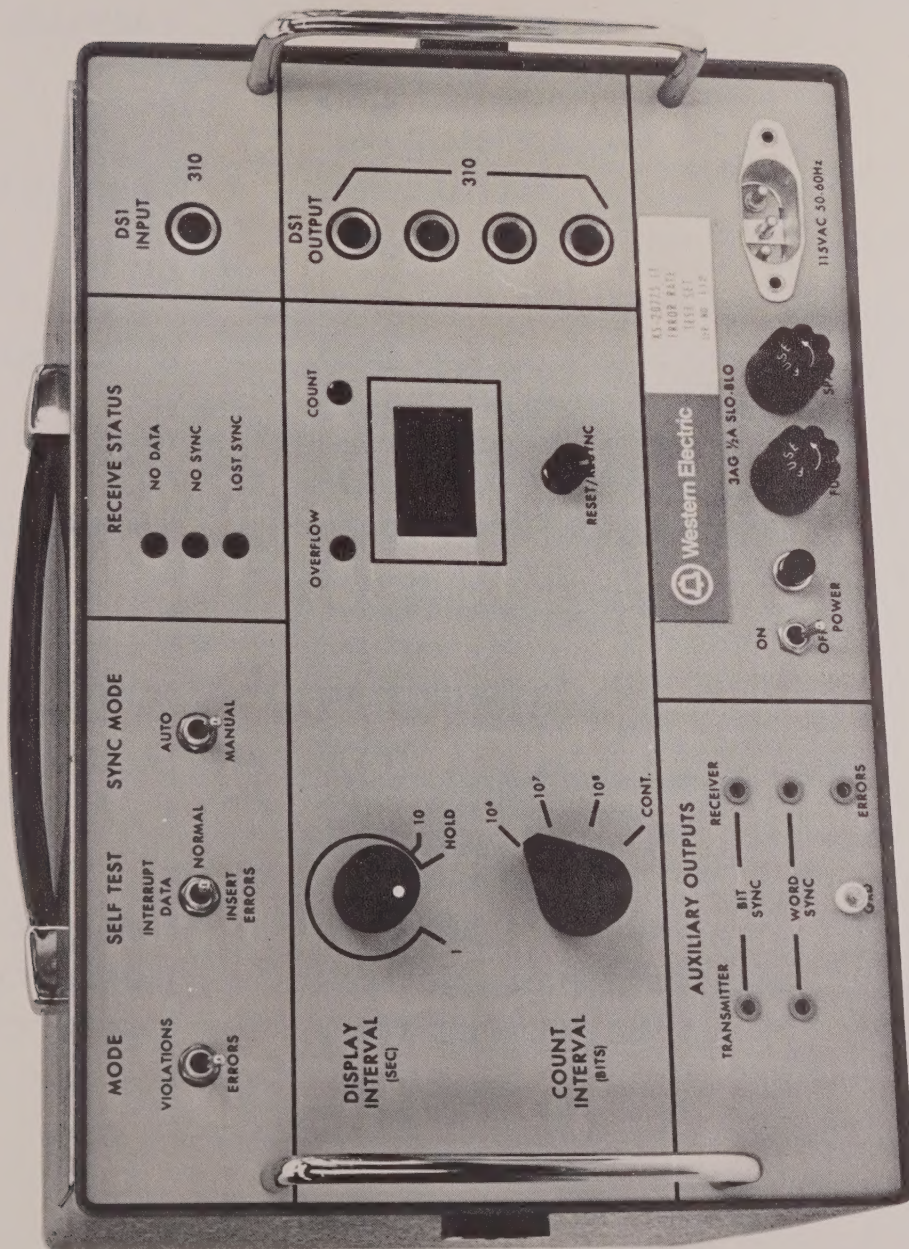
Bowmar Instrument Division
531 Main Street
Acton, Mass. 01720
(617) 263-8365



TECHNICAL MANUAL
FOR
ERROR RATE TEST SET
MODEL KS20775 L1
SERIAL NUMBER _____

MANUFACTURED BY:

Bowmar/ALI, Incorporated
531 Main Street
Acton, Massachusetts U.S.A. 01720



CONTENTS

CHAPTER 1	INTRODUCTION
1.1	Description
1.2	Scope
1.3	Specification Summary
CHAPTER 2	INSTALLATION
2.1	Preparation
2.2	Checkout
2.3	Operation
CHAPTER 3	OPERATION
3.1	Controls, Indicators and Jacks
3.2	Self Test Procedure
3.3	Applications (to be added)
CHAPTER 4	DESCRIPTION OF FUNCTIONS
4.1	General
4.2	Transmitter Circuits
4.3	Receiver
CHAPTER 5	MAINTENANCE
5.1	General
5.2	Test Equipment Requirements
5.3	Calibration Procedure
5.4	Performance Checks
5.5	Troubleshooting
CHAPTER 6	DIAGRAMS
CHAPTER 7	PARTS AND MANUFACTURERS
CHAPTER 8	SUPPLEMENTARY DATA

CHAPTER 1

INTRODUCTION

1.1 Description

The Bowmar/ALI Error Rate Test Set is a lightweight, portable instrument capable of performing a reliable check of T1 lines, T1 to T2 (M12) multiplexers, T1 to L-carrier modems, and similar digital transmission equipment. Checkout is achieved by injecting a repeating pattern of data bits from the Test Set's transmitter section to a system under test, then monitoring the system's output with a receiver section from the same or a second Test Set. The Test Set's receiver section may be set to monitor either logical errors or bipolar violations. A tally of these errors or violations, as detected over a selected interval of time, is then presented on the Test Set's numerical display.

1.2 Scope

This manual presents instrument specifications, theory of operation, drawings, and a parts list. In addition, it contains installation instructions and a maintenance section. It is intended to provide operator and technician ready reference for use of the set and for possible troubleshooting.

1.3 Specification Summary

Output Pattern

A 1,048,575 bit quasi-random pattern limited to 14 consecutive zeroes.

Input

One input, a jack to accept a WE 310 type plug.

Outputs & Jacks

A. Main: Four outputs, each a jack to accept a WE 310 type plug.

B. Auxiliary: Five outputs, each a pin jack to allow monitoring of certain signals as listed below.

1. Transmit Bit Sync
2. Receive Bit Sync
3. Transmit Word Sync
4. Receive Word Sync
5. Errors

Controls

MODE Switch	2-position: 1. VIOLATIONS 2. ERRORS
SELF TEST Switch	3-position: 1. INTERRUPT DATA (Momentary) 2. NORMAL 3. INSERT ERRORS (Momentary)
SYNC MODE Switch	2-position: 1. AUTO 2. MANUAL
DISPLAY INTERVAL (SEC)	1 to 10 seconds plus a detent setting for HOLD
COUNT INTERVAL (BITS)	4-position: 1. 10^6 2. 10^7 3. 10^8 4. CONT.
POWER Switch	2-position: 1. OFF 2. ON
RESET/RESYNC Switch	Momentary pushbutton

Indicators

Display	2-digit solid state
RECEIVE STATUS Indicators	3 separate indicators; solid state 1. NO DATA 2. NO SYNC 3. LOST SYNC
Display Status Indicators	2 separate indicators; solid state: 1. COUNT 2. OVERFLOW
POWER Indicator	1 neon lamp to show "ON" condition
Fuses	2-fuses; 3AG, 1/2 amp, Slo-Blo (1 spare)
Power	115 VAC $\pm 10\%$, 50 to 60 Hz, Single Phase
Bipolar Pulse Characteristics	
Height of Output Pulse	3V ± 0.3 V
Unbalance in height of Negative and Positive Pulse	± 0.15 V

Width of Output Pulse (half amplitude)	324 ± 30 nsec.
Unbalance in width of Positive and Negative Pulse	± 15 nsec.
Maximum rise or fall time	80 nsec.
Overshoot at trailing edge of Pulse	10 to 30% of pulse height with decay to 10% or less of base line-to-peak value within 400 nsec.
Initial Frequency Deviation of Oscillator	Within 50 Hz with Test Set at ambient temperature of 25°C.
Receiver Input Threshold	0.2 - 5.0V Peak
Sync Acquisition Time	Less than 200 Clock Pulses (Test Set shall not resync on isolated error bursts of less than 6 consecutive errors).
Operating Environment	0° to 50°C (32° to 120°F); to 95% relative humidity.

CHAPTER 2

INSTALLATION

2.1 Preparation

- a. Remove Error Rate Test Set from its packaging container.
- b. Check for presence of proper fuses (3AG 1/2A Slo-Blo).
- c. Connect power cord between Test Set and a suitable power source (115 Vac, 50-60 Hz, single phase).
- d. Set POWER switch to "ON", and note whether Power Indicator illuminates.

2.2 Checkout

Proceed with Self Test as it is outlined in Chapter 3, para. 3. 2.

2.3 Operation

When Self Test is satisfactory, proceed with desired operations. Refer to instruction decal on top of outer case for simplified operating procedures.

CHAPTER 3

OPERATION

3.1 Controls, Indicators, and Jacks

3.1.1 Input

One input, a jack to accept a WE (Western Electric Co.) #310 type of plug to pass data from the system under test to the Receiver section of the Test Set.

3.1.2 Outputs

- A. Main: Four main outputs, each a jack to accept a WE 310 type plug, are mutually independent, yet will each pass the Transmitter output to a system under test.
- B. Auxiliary: Five auxiliary outputs, each a pin jack, are provided to allow access to the signals listed below.
1. Transmit Bit Sync: The 1.544 MHz Clock signal
 2. Transmit Word-Sync: A 340 nsec pulse generated once for each cycle of the Transmitter Sequence Generator (remains high and pulls to ground level only during the 340 nsec Word-Sync-Pulse).
 3. Receive Bit Sync: The Clock signal as retrieved by the Clock Extractor circuit of the Receiver
 4. Receive Word-Sync: A 340 nsec pulse generated once for each cycle of the Receiver Sequence Generator (remains high and pulls to ground level only during the 340 nsec Word-Sync-Pulse).
 5. Errors: A pulse for every error passed by the Error Select circuitry of the Receiver (remains high and pulls to ground level only during the 340 nsec Error Pulse).

3.1.3 Controls

- 3.1.3.1 MODE Switch. A two-position toggle switch which allows selection of VIOLATIONS or ERRORS. The selection is actually for Bipolar Violations or Logical Errors. This switch instructs the Transmitter as to what type of errors to insert in the Quasi-Random Test Sequence, and it instructs the Receiver as to what type of errors to detect and count.

3.1.3.2 SELF TEST Switch. A three position momentary switch. Its NORMAL position, in the center, connects the Test Set for normal operation. With no connection to the Receiver input, the Transmitter is linked directly to the Receiver. If, at the same time, the MODE switch is set for ERRORS, all indicators will be off with no count on the Display. If the MODE switch is set for VIOLATIONS, the NO SYNC and LOST SYNC indicators are held on while NO DATA is off, and the Display shows no count.

In its INTERRUPT DATA (momentary-up) position, the bridging path between Transmitter and Receiver is opened, causing both the NO DATA and NO SYNC indicators to come on. Returning to NORMAL forces the NO DATA indicator off. If the SYNC MODE switch is at AUTO, the LOST SYNC indicator will replace NO SYNC when the switch is released.

In its INSERT ERRORS (momentary-down) position, either logical errors or bipolar violations (depending on the MODE switch setting) are injected into the Transmitter test sequence. These errors appear at the Transmitter output jacks and the Receiver input via the internal Loop Back connections. In the Receiver, these errors exercise detection and counter circuitry to be registered on the Display and serve as the self-test feature.

3.1.3.3 SYNC MODE Switch. A two-position switch. In the event that synchronization is lost, the Test Set will automatically resynchronize with the SYNC MODE Switch in AUTO position, while in the MANUAL position, synchronization must be regained by depressing the RESET/RESYNC button.

3.1.3.4 DISPLAY INTERVAL Control. A potentiometer whose setting determines the period of time the Display holds any given count. The control covers a range of 1 to 10 seconds, and at its high extreme, it may be switched into a continuous setting (HOLD).

3.1.3.5 COUNT INTERVAL. A four-position switch whose setting determines the period of time, in bits, the Counter circuits will count errors. The periods given are 10^6 , 10^7 , and 10^8 bits, with the final position allowing a Continuous tally.

3.1.3.6 RESET/RESYNC Switch. Resets the Counter, initiates a new count, resets the LOST SYNC indicator, and if in the ERRORS mode it initiates resynchronization and sets up a check of sync recognition circuits.

3.1.3.7 POWER Switch. A two-position switch which controls the application of power to the Test Set.

3.1.4 Indicators

3.1.4.1 NO DATA Indicator. A solid state indicator which is energized within 100 msec of the loss of incoming data.

3.1.4.2 NO SYNC Indicator. A solid state indicator which is energized when the Receiver is not synchronized to incoming data, or when test set is in VIOLATIONS mode.

3.1.4.3 LOST SYNC Indicator. A solid state indicator which is energized when sync is lost and subsequently recovered. This indicator goes on when sync is recovered and remains on until the RESET/RESYNC switch is actuated. If the Test Set is in the VIOLATIONS mode, LOST SYNC will be held on.

3.1.4.4 OVERFLOW Indicator. A solid state indicator which is energized when the error count exceeds the numerical capacity of the Display.

3.1.4.5 COUNT Indicator. A solid state indicator which is energized during error count intervals.

3.1.4.6 Display. A two-digit solid state indicator which presents a numerical readout of error count accumulated during any count interval.

3.1.4.7 POWER Indicator. A neon lamp which is energized whenever power is applied to the Test Set.

3.2 Self Test Procedure

3.2.1	Initial Switch Positions	
	MODE:	to VIOLATIONS
	SELF TEST:	to NORMAL
	SYNC MODE:	to MANUAL
	DISPLAY INTERVAL:	to full counter-clockwise (1 sec.)
	COUNT INTERVAL:	to 10 ⁶

3.2.2	Indicator Response	
	NO DATA:	Off
	NO SYNC:	On
	LOST SYNC:	On
	Numerical Display:	'00' at all times
	OVERFLOW:	Off
	COUNT:	On for approximately 2/3 sec., Off for approximately 1 sec.

3. 2. 3 Change DISPLAY INTERVAL control to full clockwise, but not in detent position (10 sec.). The COUNT indicator should be on for approximately 2/3 second and off for approximately 10 seconds.
3. 2. 4 Place the DISPLAY INTERVAL control in its HOLD, detent, position and momentarily operate the RESET/RESYNC button. The COUNT indicator should come on for approximately 2/3 second and then remain off indefinitely. Check the off condition for at least twenty seconds.
3. 2. 5 Place DISPLAY INTERVAL control at some point between 1 and 5 seconds. Push and hold the SELF TEST switch to its INSERT ERRORS position. The indicated count, on the Display, should change by increments of '02' from a starting count of '00' to a final count of '08' while the COUNT indicator is on. At the count of '08', the Display should hold for the period set by the DISPLAY INTERVAL control, then it should clear to '00' and begin a new cycle. The first count interval may not register a total of eight errors but each succeeding interval should yield a count of '08'.
3. 2. 6 Change the COUNT INTERVAL control from 10^6 to 10^7 , and continue holding the SELF TEST switch at its INSERT ERRORS position. The indicated count, on the Display, should perform as it did in Step 3. 2. 1. 4, above. However, the final count for a full count interval should now be '80'.
3. 2. 7 Change the COUNT INTERVAL control from 10^7 to 10^8 , and continue holding the SELF TEST switch at its INSERT ERRORS position. The indicated count, on the Display, should perform as in the preceding two steps (3. 2. 1. 4 and 3. 2. 1. 5). However, the final count for a full count interval will now be '00' and the OVERFLOW indicator should come on with the first overflow (count going from '08' to '00').
3. 2. 8 While holding the SELF TEST switch at its INSERT ERRORS position, momentarily press the RESET/RESYNC button. The Display, and the COUNT and OVERFLOW indicators should reset. A new count interval should begin within 2/3 second of release of the button.
3. 2. 9 Release the SELF TEST switch and return the COUNT INTERVAL switch to its 10^6 position.
3. 2. 10 Set the MODE switch for ERRORS, and momentarily press the RESET/RESYNC button. The Display indication should be '00' at all times, while the NO DATA, NO SYNC, and LOST SYNC indicators should be off.
3. 2. 11 Push and hold the SELF TEST switch to INTERRUPT DATA. The NO DATA indicator should come on. The NO SYNC indicator will either come on and stay on or blink rapidly and remain off. The LOST SYNC indicator may or may not come on; however, if the NO SYNC indicator is off, the LOST SYNC indicator must be on.

- 3.2.12 Release the SELF TEST switch. The NO DATA lamp should go off. The NO SYNC indicator should come on or remain on. The LOST SYNC indicator may be either on or off. The display will show '88' with an OVERFLOW indication during the count interval and any number with OVERFLOW at the end of the count interval.
- 3.2.13 Momentarily press the RESET/RESYNC button. The NO DATA, NO SYNC, and LOST SYNC indicators should remain off while the display shows '00' without OVERFLOW.
- 3.2.14 Set the SYNC MODE switch to AUTO, and hold the SELF TEST switch to INTERRUPT DATA. The NO DATA indicator should come on. The NO SYNC indicator will either come on and stay on or blink rapidly and remain off. The LOST SYNC indicator may or may not come on; however, if the NO SYNC indicator is off, the LOST SYNC indicator must be on.
- 3.2.15 Release the SELF TEST switch. The NO DATA and NO SYNC indicators should go off. The LOST SYNC indicator should come on, if not already on. The display should show '00' errors.
- 3.2.16 Momentarily pressing the RESET/RESYNC button should reset the LOST SYNC indicator.
- 3.2.17 Push and hold the SELF TEST switch to INSERT ERRORS. The display should change by increments of '02' to a final count of '08'.

3.3 Application

- 3.3.1 The Error Rate Test Set can be used to test any digital transmission system or system component accepting a DS-1, T1-type, bipolar signal and returning a similar signal. While the receiver of the ERTS is equivalent in application to bipolar-violation detectors for testing T1 lines, its bit-by-bit error detection, using a long pseudo-random sequence, is particularly intended to test those system components which remove bipolar violations and/or are capable of causing logical errors without causing violations. The transmitter of the Error Rate Test Set is equivalent to and interchangeable with the Bell System's J98710R T-1 Quasi-Random Signal Source and may be used independently of the receiver for end-to-end tests or as a portable source. While the transmitter provides a 3 volt bipolar signal for input at the cross-connect bay, the receiver may operate at or up to 750 feet from the cross-connect bay or similar source, or at the Monitor jack. The following gives specific applications of the Error Rate Test Set in testing T1 lines, T1 to T2 (M12) multiplexers and modems.
- 3.3.2 The Error Rate Test Set may be used to test any T1 line using either its bipolar-violation or logical-error detection schemes. The only constraint on the choice of detection is that logical-error detection requires the use of the standard test sequence whereas bipolar-violation detection may be applied to any signal. An example of the better type of detection using message/data as the signal would be the in-service monitoring of a circuit without the necessity of removing it from service. Figures 1A and 1B

depict typical applications of the Error Rate Test Set for checking T1 lines in both loopback and end-to-end configurations.

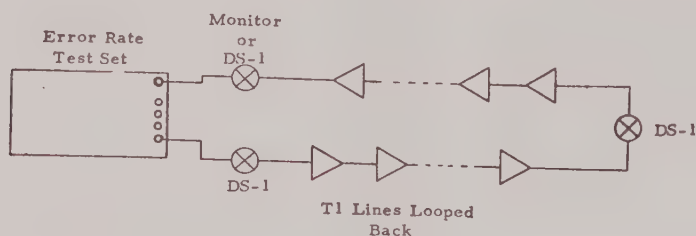


Figure 1A

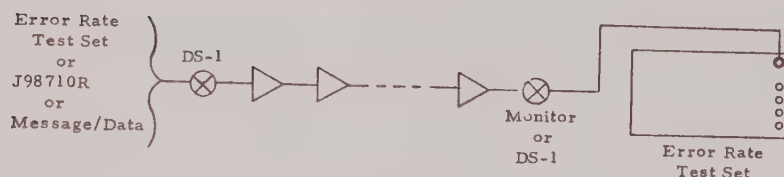


Figure 1B

3.3.3 In some instances, idle circuits in an office may carry the standard test pattern merely to provide signal excitation. Therefore, in order to verify circuit identification, the Error Rate Test Set used as the signal source may be instructed to insert a fixed rate of either logical-errors or bipolar-violations into its sequence. The rate is approximately 8×10^{-6} and, added to the actual errors, such an increase in rate can be recognized on most circuits.

3.3.4 Multiplexers and modems interfacing DS-1, T1, signals to either higher order digital systems or analog systems are capable of removing bipolar violations from their inputs and/or can cause logical-errors without violations appearing in the output data. The pseudo-random sequence and logical error detection makes it possible to evaluate such systems. As an example, consider the DS-1 to DS-2, T1 to T2, multiplexer (M12) which combines four DS-1 data streams into one DS-2 stream. While the test sequence is needed only for the channel under check, the Error Rate Test Set provides four identical outputs to identically stress all four channels of the multiplexer. Not only are loopback and end-to-end tests possible, but tests over the higher order system or analog medium are also possible as depicted in Figures 2A and 2B.

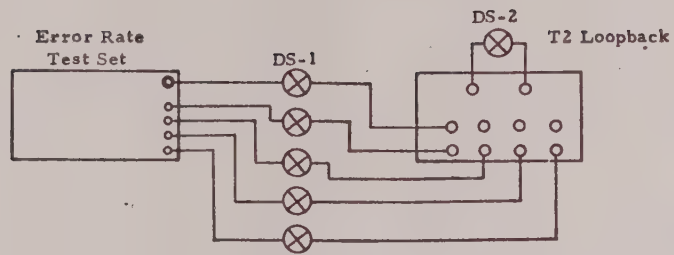


Figure 2A

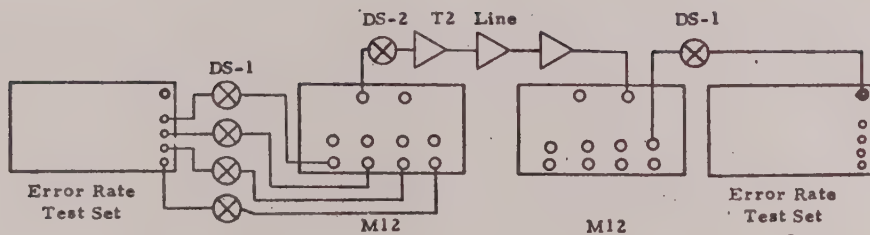


Figure 2B

CHAPTER 4

DESCRIPTION OF FUNCTIONS

4.1 General

Refer to the Block Diagram (Figure 4-1) and to schematics of Chapter 6 to correlate descriptions offered in this chapter.

4.1.1 Transmitter

The Transmitter section of the Error Rate Test Set is a DS-1 (T-1) type test source. Its output is a continuously repeating sequence of data bits in a quasi-random arrangement identical to that provided by Bell System test sources (Western Electric J98710R T-1 Quasi Random Signal Source).

The output supplied by each of four independent jacks is a 1.544 Mbps, 3 volt, bipolar, return-to-zero signal with trailing edge overshoot. It is derived from a 1,048,575 bit Sequence Generator which is self-starting and it is limited to fourteen consecutive zeroes even though the Sequence Generator produces longer strings of zeroes at several intervals.

For purposes of self-test and the test of other systems, the Error Rate Test Set can be made to insert a fixed number of errors into each cycle of the Transmitter test sequence. A front panel switch offers a choice of either logical errors or bipolar violations. Their insertion depends on the detection of seventeen or more consecutive zeroes in the internal pattern of the Sequence Generator. Since the required condition of zeroes occurs four times per cycle of the test sequence, there are four pairs of errors inserted.

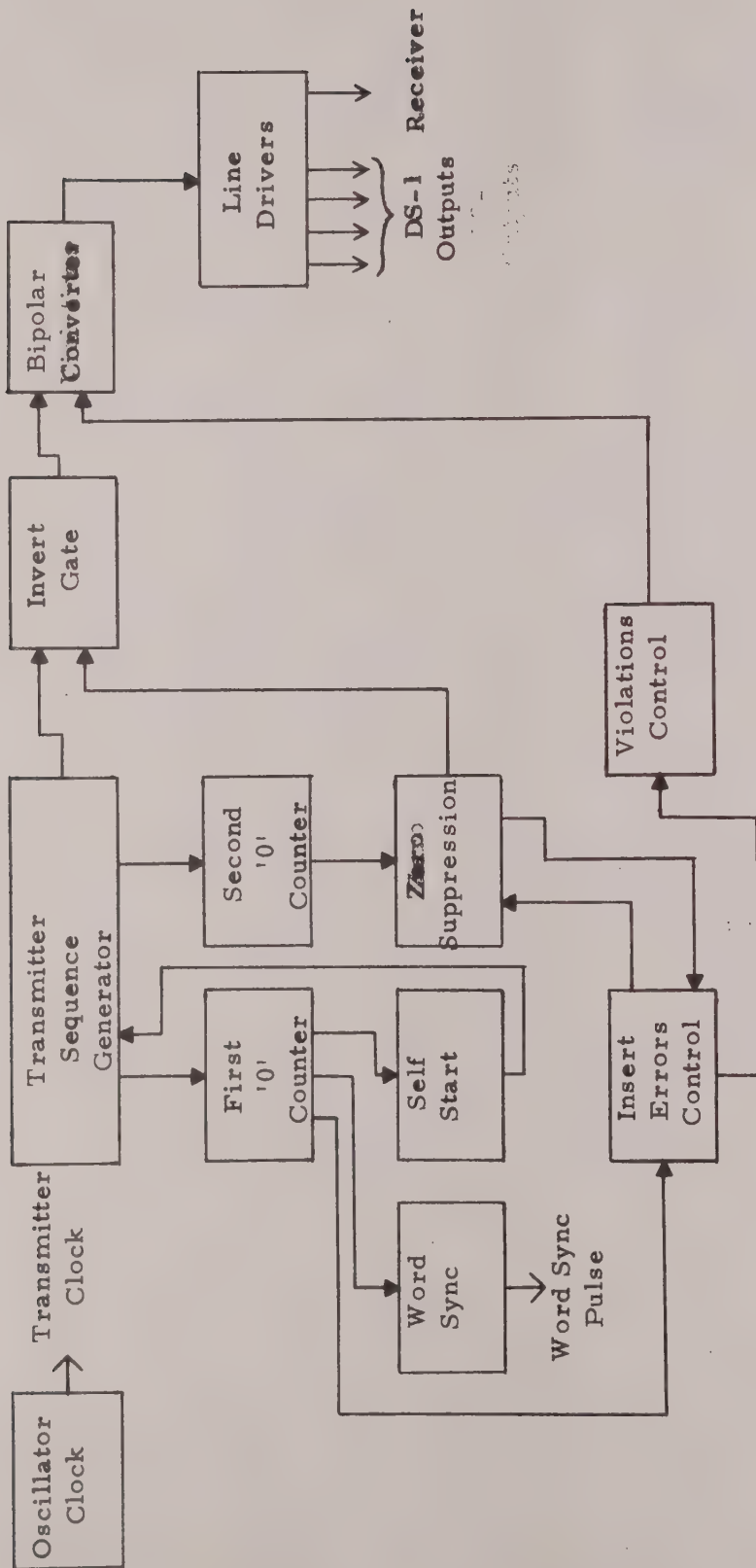
Logical error insertions of a zero-to-one and a one-to-zero conversion are performed by altering the function of the circuit which limits the output sequence to a maximum of fourteen consecutive zeroes. This alteration is accomplished without violating either the fourteen-zero restraint or the bipolar format.

Bipolar violations consist of four consecutive ones, the first two of one polarity, and the second two of opposite polarity. This is accomplished by inhibiting the Bipolar Generator which normally alternates the polarity of each consecutive one (whether or not they are interspersed with zeroes

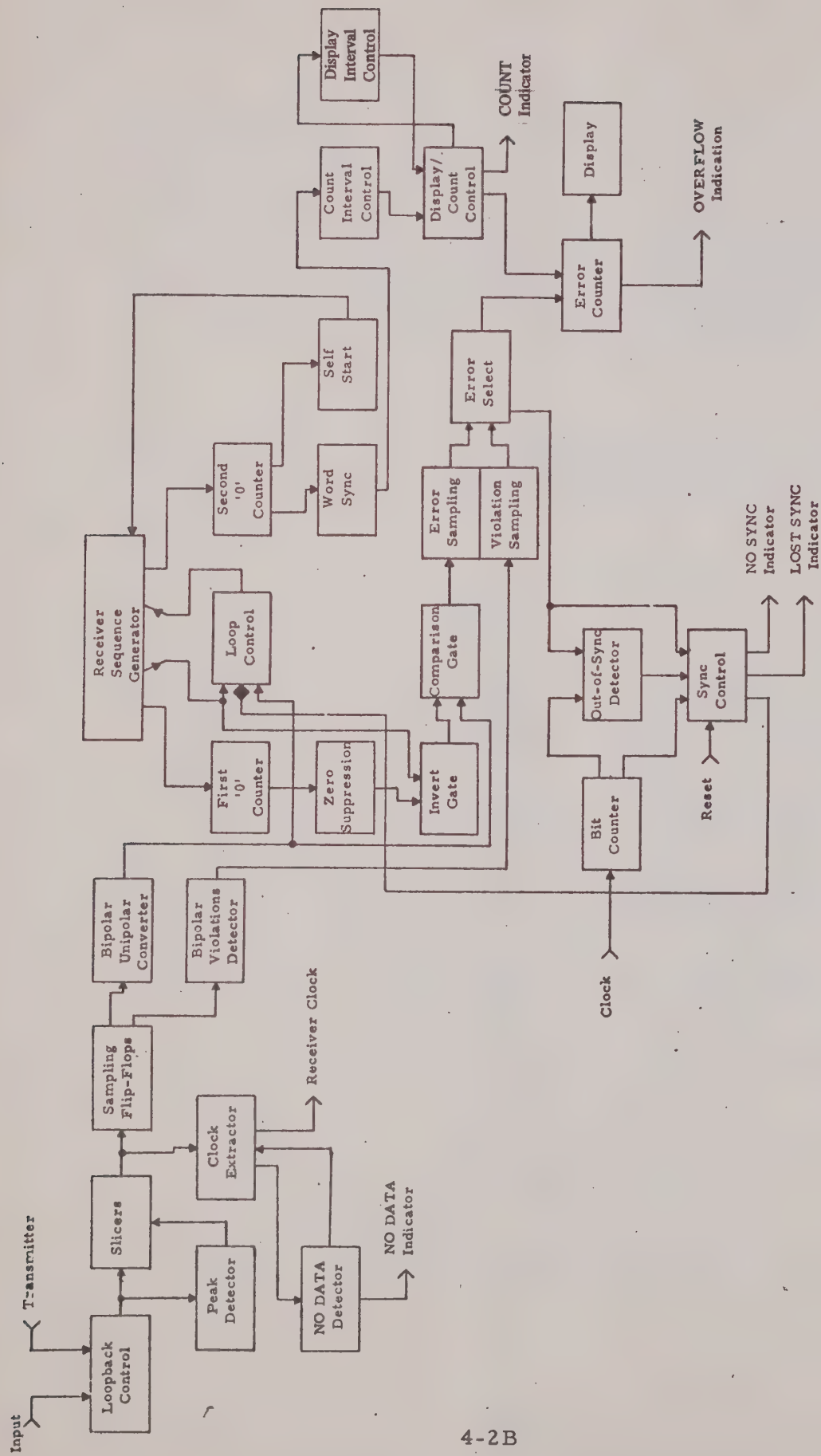
The first three, four, or five zeroes of the seventeen-or-more zero-condition-for-errors are thus forced to ones.

The chart below illustrates a typical condition of seventeen or more zeroes in the Sequence Generator. The Transmitter normally suppresses all zeroes in excess of fourteen by means of circuitry at the output of the Sequence Generator. However, when error insertion is desired, the normal functions of these added circuits ~~is~~ altered to inject the errors as shown.

Description	Data Stream Segment
Any condition of 17 or more zeroes (18 shown) in Sig. Gen. output:	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
Corrected output (without errors):	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
Corresponding Xmitter Output, Bipolar Format:	+ - + - + 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 -
Corrected Sig. Gen. output with Logical Errors:	0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
Correspond Xmitter output, Bipolar Format: Errors:	0 + - + - + 0 0 0 0 0 0 0 0 0 0 0 0 0 0 - X X
Corrected Xmitter output with Bipolar Violations: Violations:	+ + - - + 0 0 0 0 0 0 0 0 0 0 0 0 0 0 - X X



Block Diagram of Transmitter Section
Figure 4-1A



Block Diagram of Receiver Section

Figure 4-1B

4. 1. 2 Receiver

Evaluation of data from a system under test takes place in the Receiver section of the Error Rate Test Set. Incoming data, in its bipolar format, is first sliced about its half peak amplitude point and subsequently sampled at the center of the bit period. A Peak Detector provides automatic threshold control for the slicers.

Clock pulses for the Receiver are taken directly from the reshaped data by a Clock Extractor circuit. In the event that data is discontinued, a No-Data Detector linked to the Clock Extractor signals the No-Data indicator on the front panel and inhibits clock pulses to the following circuitry.

Reshaped and Sampled data is directed to the Bipolar Violations Detector. In normal bipolar data, each consecutive one is alternated in polarity, whether or not there are zeroes in between. When two consecutive ones have the same polarity, the second is considered an error, and bipolar format has been violated. The output of the Bipolar Violations Detector is then ANDED with the output of the Bipolar/Unipolar Converter. This latter circuit has converted the bipolar data from the Sampling circuit to a unipolar format.

If the front panel MODE switch is set at VIOLATIONS, the output from the Bipolar Violations Detector is forwarded to Error Count circuits for subsequent display. The sequence generator of the receiver, described below, continues to cycle solely for the purpose of providing a time base for test length selection via the COUNT INTERVAL switch. When operating in this capacity, the sequence generator is self starting but is not allowed to attempt to synchronize to the received data stream.

If the front panel MODE switch is set at ERRORS, the count from the Bipolar Violations Detector is ignored. Instead, the unipolar data stream is routed to the Receiver Sequence Generator. This generator differs from its transmitter counterpart only in its monitor points, and in a modified feedback loop. Otherwise, it is capable of the same 1, 048, 575 bit test pattern.

The key difference between Transmitter and Receiver Sequence Generators is the latter's modified feed back loop. This loop is arranged to be opened or closed. In its closed mode, the Receiver generator behaves exactly like the Transmitter generator; it is a self-starting generator for the 1,048,575 bit test sequence. In its open mode, however, it is injected with the received test pattern in unipolar format. If the received test pattern is without error, it will deceive the generator into behaving as a closed loop device, thus synchronizing the generator to the received pattern.

The self-synchronizing feature of the Receiver Sequence Generator may be initiated automatically or manually, depending on the setting of the SYNC MODE switch (two settings: AUTO or MANUAL) on the front panel. In the MANUAL mode, loss of sync is indicated by the NO SYNC indicator; resynchronization may be gained by pressing the RESET/RESYNC button.

Once Sequence Generator sync is achieved and the loop is again closed, received data is compared with the Generator output for logical errors. Error signals are then directed to the Error Counter for subsequent display. As with violations, the Display will show errors per cycle of the test sequence, or per ten or one hundred cycles depending on the setting of the COUNT INTERVAL switch. The exception to errors per cycle(s), for both logical errors and bipolar violations, will be a cumulative tally made when the COUNT INTERVAL switch is at its "CONT" setting.

4.2 Transmitter Circuits

4.2.1 1.544 MHz Clock

A 3.088 MHz crystal oscillator is divided by a single JK flip-flop to provide a 1.544 MHz symmetrical, two-phase clock. Transistors Q1 and Q2 make up the oscillator, with Q3 and Q4 serving as an emitter-follower and a buffer. Q1 and Q2 are connected as a two-transistor amplifier with negative feedback. Q1 provides most of the gain. Negative feedback stabilizes the bias points and holds crystal current to a good operating range. Positive feedback through the crystal is sufficient to produce oscillation. Oscillation occurs at the frequency of minimum crystal impedance, the series-resonant frequency. The oscillator output is divided by IC17A. Resultant clock pulses are distributed throughout the Transmitter to control all timing functions.

4.2.2 Transmitter Sequence Generator

Quasi-random test patterns, or sequences, issued by the Transmitter are derived from a 20-stage shift-register generator whose feedback is taken

from stages 17 and 20. The Generator is contained by I. C.'s 1A through 4B, with feedback directed through the exclusive-or circuit of IC8B.

The Generator provides a continuously repeating sequence of 1's and 0's. Each sequence is made up of all but one of the 2^{20} possible combinations of 20-bit states, for a total of 1,048,575 bits. The one exception is the all-zero state in which the Generator will not function. When the all-zero state does occur, it is eliminated by a Self Start circuit (see Section 4.2.4). Each resultant sequence therefore contains strings of 1's up to and including 20 bits and strings of 0's up to and including 19 bits.

The main output of the Generator is taken from the 20th stage. Additional outputs are taken from the 2nd, 5th, 6th, and 7th stages. These auxiliary outputs enable sequence bits to be monitored during their serial progression through the chain of register stages. The bits shift a stage at a time with each Clock pulse.

The sequence monitored at the auxiliary outputs is the same as that issued at the main output. However, where each auxiliary output is some number of stages ahead of the main output, the sequence at each auxiliary output is the same number of bit periods ahead in time of the sequence at the main output. This feature allows a "pre-view" of the output for purposes of possible correction or alteration in subsequent circuits. Specific purposes of the auxiliary outputs are described in the sections that follow.

4.2.3 Transmitter '0' Counters

Two separate counters are connected to auxiliary outputs of the Sequence Generator to register any series of successive 0's. Both counters are actually incremented by Clock pulses, but each is reset by registration of a 1 so that effectively they are counting 0's.

The first counter is a 5-bit binary counter connected to the 2nd-stage output of the Sequence Generator. It is used to aid the Self Start circuit (see Section 4.2.4), to provide a sync pulse at the beginning of the test sequence, and to control the injection of errors. Its components are IC's 13A, 5A, and 7A.

The second counter is a 4-stage counter contained by IC6A. It is connected to the 5th-stage output of the Sequence Generator and at this tap it is 3 bits behind the 2nd-stage tap. This counter signals the Zero Suppression Control (see Section 4.2.7) when it has registered fifteen consecutive 0's in the test sequence. Thus, the number of 0's delivered to the line or device under test may be limited. This limitation is imposed without disturbing the contents of the shift register.

4. 2. 4 Transmitter Self Start Circuit

Self starting is initiated by a single gate, IC10A, which is activated by a count of 24 from the First '0' Counter (see Section 4.2.3). This count is possible only if the Sequence Generator is in the all-zero state.

As described in Section 4.2.2, all-zeroes in the Sequence Generator is an illegal state in which the Generator cannot function. Upon registration by the First '0' Counter of 24 0's, the Self-Start circuit is activated to force a single 1 into the Sequence Generator. Appearance of the 1 cancels the illegal state and stimulates the Generator into normal operation.

4. 2. 5 Transmitter Word Sync Circuit

The Word Sync Circuit consists of a single gate, IC9B, used in conjunction with an inverter, IC13D. It is connected to the First '0' Counter to respond to the passage of 19 0's followed by a 1 through the Sequence Generator. Since this condition occurs only once every 1,048,575 bits, it is used to mark each full cycle of the Sequence Generator. The Word Sync Circuit responds to this count by providing a sync pulse to a front panel test point.

4. 2. 6 Insert-Errors Control

Error injection into the test sequence is initiated by holding the SELF TEST switch at its INSERT ERRORS position. Errors may be logical or they may be bipolar violations, depending on the MODE switch setting (the MODE switch offers two settings: VIOLATIONS or ERRORS).

Errors are forced into the test sequence after its issue by the Sequence Generator. Insertion is triggered by the First '0' Counter's detection of seventeen or more consecutive 0's, counted as they pass through the Sequence Generator. This condition occurs four times during each cycle of the test sequence. In each instance, a pair of errors, rather than a single error, is inserted so that both a 1-to-0 and a 0-to-1 conversion is accounted for. Thus for each cycle of the test sequence, four pairs of errors may be injected.

Insert-Errors Control circuitry is made up of several gates, inverters, and a single flip-flop. These are IC's 9A, 13C and E, 14D, 15A, 18A through C, and 19A through C. IC15A is the lone flip-flop. The count of seventeen 0's is detected by IC9A and used to set the flip-flop. The remaining gates then act as steering circuits enabling the Insert-Errors Control to interact with either the Zero Suppression Control or the Violations Control (Sections 4.2.7 and 4.2.8 respectively) in the forcing of errors.

4. 2. 7 Zero Suppression Control

The Second '0' Counter being a 4-stage device, as described in Section 4. 2. 3, it can count up to fifteen 0's. The test sequence, as furnished at the Test Set output, is intended to contain no more than fourteen consecutive 0's. Therefore, when the Second '0' Counter registers its fifteenth consecutive 0, it activates the Zero Suppression Control to convert all excess 0's at the Sequence Generator's output to 1's.

The Zero Suppression Control is made up of gates, inverters and a flip-flop. These are IC's 10B, 11A through D, 14A through C, and 15B. The flip-flop is IC15B.

The Second '0' Counter taps the 5th stage of the Sequence Generator. Its count is therefore fifteen bits ahead of the Generator's output at the 20th stage. By the time the Counter records the fifteenth 0 of a string, the first 0 of the same string is at the Generator's output. At the same time, the gate of IC10B detects the count of 15 and signals the Zero Suppression Control into action. The Zero Suppression Control responds by converting the first and subsequent 0's of the string to 1's. Zero-to-one conversion continues until a 1 is detected at the 6th stage tap of the Sequence Generator. The appearance of a 1 at the 6th stage tap turns off the Zero Suppression Control, and the last fourteen 0's of the string are allowed to pass.

Operation of the Zero Suppression Control is modified slightly when logical errors are to be inserted. As discussed in Section 4. 2. 6, errors are inserted when the Sequence Generator contains seventeen 0's. However, a signal from the Insert-Errors control and the First '0' Counter turns on the Zero Suppression Control one bit earlier than normal. In this way, the bit preceding the string of 0's at the Sequence Generator output is converted to a 0, thus providing an error of the 1 to 0 conversion type. In addition, steering gates in the Insert-Errors Control switch the Zero Suppression Control turnoff from the 6th stage to the 7th stage of the Sequence Generator, thus turning off the Zero Suppression one bit later than normal and forcing an extra zero-to-one conversion. This conversion is also an error. The net result for the seventeen 0 string is therefore two errors, a 1 to 0 and a 0 to 1 conversion.

The following chart provides a visual representation of Sequence Generator contents and output, with and without error pairs.

Sequence Generator	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Normal Output	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
Output With Errors	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
	#1 error				#2 error													
	Time																	

4.2.8 Bipolar Violations Control

The Bipolar Violations Control, consisting of IC's 21A and 12B, acts upon instructions from the Insert-Errors Control to inject violations into the Test sequence data stream. This is accomplished by disabling the Bipolar Generator (Section 4.2.10) for the appropriate bits of the data stream.

IC's 21A and 12B make up a 3-bit binary counter and a sampling flip-flop, the latter for timing adjustment purposes. When violations are to be inserted, per actuation of the SELF TEST and MODE Switches, the 3-bit counter commences to register Clock pulses. The output of the counter's first stage is then connected to inhibit the Bipolar Generator, which is presented a string of forced '1's' during this process. The Bipolar Generator is inhibited after the counter's first 1, enabled after the second, and inhibited again after the third. When the counter registers a count of 4, the Insert-Errors Control and Bipolar Violations Control are both reset.

During each 4-bit operating period, the Bipolar Violations Control causes two consecutive 1's of one polarity followed by two consecutive 1's of the opposite polarity. These constitute an error-pair. As discussed in Section 4.2.6, there are four error-pairs per test sequence. Bipolar violations are inserted without causing logical errors.

4.2.9 Invert Data Gate

IC8A is an exclusive-or gate through which the Zero Suppression Control inverts output bits of the Sequence Generator. The inversion forces each 1 to a 0 and each 0 to a 1.

The output of IC8A is sampled and delayed one-half bit by IC12A. This delay eliminates transients which result from simultaneous switching of the many circuits controlled by Clock pulses. The output of the sampling flip-flop is then "ANDED" with Clock pulses through IC16A to obtain a return-to-zero data format for the Bipolar Generator (Section 4.2.10).

4. 2. 10 Bipolar Generator

A single flip-flop, IC7B, and four gates, IC's 16C & D and IC8C & D make up the Bipolar Generator. Its function is to alternate the polarity of all 1's in the test sequence regardless of the interspersions of 0's. Thus, when a 1 is generated with one polarity, the next 1 will have the opposite polarity whether or not there are 0's between the two 1's.

Bipolarization is triggered by the trailing edge of each 1 in the data stream. At this instant, the flip-flop of IC14 toggles so that the next 1 is transmitted with the opposite polarity. Two gates, IC8C & D, delay the toggle input to the flip-flop slightly to insure a correct time relationship with the inhibit input from the Bipolar Violations Control circuit.

The output of the Invert Data Gate is "ANDED" with each of the toggle flip-flop outputs to provide necessary steering for the Line Drivers (Section 4. 2. 11). Where a bipolar violation is to be inserted, the 1 to be transmitted is of the same polarity as its predecessor. The toggle flip-flop must not operate during transmission of this violation. During transmission of a bipolar violation, the toggle flip-flop is therefore momentarily disabled. The required disability is imposed by the Bipolar Violation Control, as described in Section 4. 2. 8.

4. 2. 11 Line Drivers

Each of the Bipolar Generator's two outputs is directed to a paralleled pair of driver transistor switches whose outputs are tied to an outer tap of a center-tapped transformer primary. The paralleled transistor switch arrangement ensures a higher speed of operation and higher current capacity. One switch pair with half the primary handles positive bits of the bipolar signal while the other pair and half handle the negative bits.

The Transformer is trifilar wound with two of its windings connected as the center-tapped primary. The third winding serves as the balanced output, padded as necessary and distributed to the front panel jacks and to the receiver.

Shaping of the inherently square signal bits into T1 pulse shape with trailing edge overshoot is accomplished with a passive RLC circuit. The RLC circuit is connected across the transformer primary.

4. 2. 12 Pads

The output of the Line Drivers is connected to a parallel arrangement of pads which serve to drop output voltage to three volts while providing a measure of isolation between outputs. Four pads link the line drivers to front panel jacks. A fifth pad of higher attenuation provides a loop back path from the Transmitter to the Receiver sections for self test purposes.

The output of each of the five pads is arranged to terminate in 100Ω if it is not in use. This presents a constant impedance to the Line Drivers and pulse-shaping network, regardless of the number of outputs in use.

4.3 Receiver

4.3.1 Loop Back Control

A reed relay (K1) and its coil driver (Transistors Q1 and Q2) are used to open or close the bridge between Transmitter and Receiver. The bridge is closed unless a plug is inserted into the Receiver input jack, or unless the SELF TEST switch is held at its INTERRUPT DATA position. In its open position, the relay is de-energized.

4.3.2 Peak Detector

To accommodate bipolar inputs of widely varying amplitudes, a Peak Detector circuit supplies a threshold level to the Slicers (Section 4.3.3). This circuit is a full-wave type which effectively converts its bipolar inputs to unipolar. Its output is taken from a voltage divider which, coupled with capacitor (C3), supplies a level half the peak amplitude of each incoming '1' bit. Transistors Q3 and Q4 and divider resistors R10 and R11 make up the Detector.

4.3.3 Slicers

A pair of Slicer circuits compares the outputs from the two Transformer T1 secondary extremities to the output of the Peak Detector to establish a peak level for each incoming '1' bit. Bits of one polarity are handled by Transistor Q5 in conjunction with IC5A and B, while the opposite polarity uses Q6 and IC5D and C. A separate output for both polarities preserves the polarity information for the violation detector. The entire function is performed by a dual-high-speed line receiver which gives high speed operation with little offset error.

4.3.4 Clock Extractor

In order that the Receiver can properly synchronize with incoming signals, it derives clock pulses from incoming data rather than an internal clock. The Clock Extractor monitors and effectively rectifies both Slicer outputs through IC6A and Q7. The rectified signal is then converted into a series of pulses, one for each '1' bit, which are applied to a very high-Q-circuit. The result is a ringing output of more than adequate duration to supply clock pulses during strings of '0' bits of the maximum allowable length. Thus, a 1.544 MHz frequency component is extracted from the received signal regardless of '0' bits.

The output of the high-Q-circuit is phased as required and applied to a separate slicer for shaping. The output of the slicer is directed to IC7B together with the output of the No Data Detector. The output of IC7B is a symmetrical clock signal of proper phase for the entire receiver. This output is inhibited when No Data is detected to prevent the tally of errors due to this condition.

4.3.5 No Data Detector (Unit with -202 Receiver Board Assembly)

This circuit is a peak detector which monitors the Clock Extractor. In the absence of data, it provides signalling to the NO DATA indicator and to the output of the Clock Extractor to clamp this output. The output of the Clock Extractor is sliced by comparators (IC7A and D) to provide a logic level signal for the NO DATA indicator.

No Data Detector (Unit with -212 Receiver Board Assembly)

This No Data Detector, consisting of IC9 monitors the output of the slicers through IC6A. The dual retriggerable monostable multivibrator IC9 is connected in a tandem arrangement, where the second stage is triggered by an output of the first. The first stage is continuously retriggered by data pulses from the output of IC6A. In the event that data is interrupted, retriggering is discontinued, permitting this stage to complete its monostable function. The time constant of the first stage (26.5 microseconds) is determined by circuit elements R57 and C26. This time constant corresponds to 41 ± 9 zeroes, which defines the No Data threshold. The second stage, when triggered by the No Data condition detected by the first stage, generates a pulse of 100 ± 20 ms. An output from this stage is applied to the gate input of the first stage which inhibits triggering of the first stage for a 100 ms period following detection of No Data. The 100 ms time constant is determined by components R56 and C27. The output of the No Data circuit is extracted from the first stage. This output is directed to both the No Data indicator buffer through IC6D and to the clock extractor circuit IC7B.

4.3.6 Bipolar/Unipolar Converter

Positive and negative data bits are carried by their own separate lines from their respective slicers to D-type sampling flip-flops. (IC's 1A and B). The flip-flop outputs are OR'ed by IC3A to be converted to a single, unipolar, NRZ (non-return-to-zero) signal.

4.3.7 Bipolar Violations Detector

This circuit consists of a pair of two-stage binary counters, IC's 2A and B for one and IC's 4A and B for the other. A gate for each counter AND's the Receiver Clock pulses with a slicer output to give return-to-zero signals which toggle and reset the counters.

When a '1' of positive polarity is received, the first stage of one counter is set while the other counter is cleared. When a '1' of negative polarity follows, the first counter is cleared while the second is set for a count of 1. Should two '1's of the same polarity arrive, one of the counters will register a count of 2 to indicate bipolar violation.

OR'ing the two counter outputs and AND'ing the result with the unipolar data stream completes the bipolar detection process. This arrangement enables detection of violations even though the consecutive 1's are separated by one or several 0's. It also allows registration of a string of bipolar violations. The resultant violations data is channelled to the Error Counters for subsequent display, provided the MODE switch is set for VIOLATIONS.

4.3.8 Receiver Sequence Generator

Should the MODE switch be set to ERRORS, incoming data as processed by the Bipolar/Unipolar Converter is directed to the Receiver Sequence Generator and associated circuits whose purpose is the detection of logical errors.

The Receiver Sequence Generator produces a test sequence identical to that of the Transmitter Generator. However, the Receiver Generator differs somewhat in configuration. First, its outputs are taken from different stages. Second, its timing is derived by extracting clock pulses from incoming data rather than an internal clock. Finally, its feedback loop may be opened to receive incoming data rather than its own output for the purpose of synchronization.

The intent of different output locations is explained in sections that follow, while clock-pulse extraction is accounted for in Section 4.3.4. This leaves, then, manipulation of the feedback loop.

With the feedback loop closed, the Receiver Generator behaves exactly as the Transmitter Generator in working up the 1,048,575 bit test sequence. But it is necessary to synchronize the test sequence from the Receiver Generator with that of an incoming signal if a bit-by-bit comparison of data bits is to be performed. This synchronization is achieved by opening the feedback loop and inserting the incoming signal in place of the Generator's output. The Generator responds as if the loop were closed, and within a very brief time interval (20 data bits later) the Generator's output corresponds exactly with the data being inserted in its place.

Should incoming data contain error bits during synchronization, the process will be delayed. In order for synchronization to be achieved, incoming data must contain at least 20 error-free bits. An additional 40 error-free bits must be received in order to confirm resynchronization. And once synchronization is confirmed, the Generator's Sync Control circuit (Section 4.3.19) forces the feedback loop to its closed status so that normal operation may resume.

Should synchronization be lost during normal operation, the loss is detected by the Out-of-Sync Detector (Section 4.3.18). In the auto sync mode, this circuit then signals the Sync Control to re-open the feedback loop for resynchronization. Resynchronization can also be initiated by depressing the RESET/RESYNC button.

Generator components are IC's 1A and B, 2A and B, 3A, and 4A. IC11B serves as the exclusive-or circuit in the feedback link. The Generator's output is taken from IC4A, which is stage 17. And the bridge between stages 17 and 18 contains the Loop Control circuitry (Section 4.3.9) which opens or closes the feedback loop.

4.3.9 Loop Control

The gate system, made up of IC's 8A, -B, and -C, effectively forms a SPDT switch which controls the Receiver Generator's feedback loop. The input to stage 18, from IC8B, is the common line. In one mode, stage 18 receives data directly from the output of stage 17, while in the other it receives the incoming, unipolar data signal. IC6E is an inverter through which the Sync Control (Section 4.3.19) may force the Loop Control to switch stage 18 to the incoming data line, should synchronization be required. If the Generator is properly synchronized to incoming data, there will be no signal from Sync Control; the Loop Control will therefore switch data from stage 17 to stage 18.

4.3.10 Receiver '0' Counters

Two '0' Counters are connected to the Receiver Sequence Generator. Their functions and operation are identical to those described for the Transmitter.

The first counter monitors the output of stage 1. It is a 4-bit binary counter used in limiting the number of consecutive 0's in the Receiver Generator's test sequence and is contained in IC5A.

The second counter is a 5-bit affair connected to the Generator's stage 19 output. It serves in the generation of a "word-sync-pulse" (Section 4.3.12) and to make the Generator self-starting for bipolar violations measurements. (For bipolar violations measurements, the Generator serves only in the making of a word-sync-pulse for each cycle of the test sequence.)

4.3.11 Receiver Self-Start Circuit

Operation and function of this circuit are identical to its Transmitter equivalent. It differs in its interfacing, however, in that its input is taken from the Second '0' Counter, and its output is routed to the Generator's 19th stage. The IC8D gate is the entire circuit.

4.3.12 Receiver Word-Sync Circuit

The Word-Sync Circuit is also a duplicate of its Transmitter counterpart. Its input gate, IC7B, is connected to the Second '0' Counter, while its output is directed through inverter IC12D and Transistor Q10. The output is also routed to the Display/Count Control and the Count Interval Control. In the latter circuitry, the Word-Sync pulse serves as the major time base.

4.3.13 Receiver Zero-Suppression Circuit & Invert Data Gate

Input gate IC7A, of the Zero Suppression Circuit, is connected to monitor the First '0' Counter for a count of fifteen 0's. A second input is taken from the 3rd stage of the Sequence Generator to serve as a reset line for the Suppressor's flip-flop, IC10A.

As does its Transmitter namesake, the Zero Suppressor limits consecutive 0's from the Sequence Generator to a total of fourteen. While more than fourteen 0's may be generated, the first fifteen are registered by the First '0' Counter. Input gate IC7A responds to the count of fifteen by setting IC10A with a signal delivered through IC's 12B and C and 13A. At the same instant IC10A is set, the last 1 prior to the string of 0's is issued from the main output, stage 17, of the Sequence Generator.

When IC10A is set, all 0's issued from the Generator are converted to 1's by Invert Gate IC16A, while all 1's are maintained. Thus, the last 1 issued prior to the string of 0's is kept intact while all 0's that follow are converted to 1's. This process continues until appearance of a 1 at the Generator's 3rd stage output. A 1 at the 3rd stage output resets IC10A. The remaining 0's, one in each of the following Generator stages are allowed to pass. Since there are fourteen stages between stage 3 and the main output at stage 17, only fourteen 0's are actually issued without conversion. Thus, consecutive 0's from the Generator are limited to fourteen in all.

4.3.14 Invert Data & Comparison Gates

IC16A is merely a NAND gate used for an OR function. Since the Receiver requires only 0-to-1 conversions, and not the 1-to-0 conversions used by the Transmitter, an exclusive-or gate is unnecessary. The output of the Invert Data Gate is not sampled, as in the Transmitter, but is passed directly to the Comparison Gate.

The Comparison Gate, IC11A, is an exclusive-or used to compare the received-data-stream, from the Bipolar/Unipolar Converter, with the test pattern from the Sequence Generator. Comparison is performed bit-by-bit, and any differences appear as logical ones at the output of the Comparison Gate.

4.3.15 Sampling Flip-Flops

The output of the Comparison Gate and the output of the Bipolar Violations Detector are sampled by D-type flip-flops IC15A and IC15B respectively. Thus, detected logical errors and bipolar violations are simultaneously available to the Error-Select Circuit (see below). These error signals are provided in NRZ (Non Return to Zero) format.

4.3.16 Error-Select Circuit

The outputs of both Sampling Flip-Flops connect to Error-Select Circuit gates IC13B and IC14B, where they are AND'ed with Clock pulses. By ANDing the Sampled outputs with Clock pulses, their NRZ format is converted to RZ format, or a separate pulse for each error, by the Error-Select input gates.

Bipolar violations can be ANDed with Clock pulses at the Error-Select input gate only when the Mode switch (front panel) is set to "Violations". Logical errors, however, are ANDed with Clock pulses at the corresponding input gate whenever they appear. The resulting logical error pulses are inverted then directed to a second gate, IC13C. At this point they are also directed

to the Out-of-Sync Detector and to the Sync Control, which function normally regardless of the position of the mode switch. Passage of logical error pulses through the second gate, IC13, is then dependent on Mode switch setting. Thus, either the passage of bipolar violations through Error-Select gate IC14B or the passage of logical errors through Error-Select gate IC13C depends on the Mode switch setting.

From the selectable gates either error signal is ORed through IC13D to the gate IC14C. Passage through IC14C to Counter circuitry then depends on signals from the Display/Count Control.

4.3.17 Bit Counter

The Bit Counter is made up of IC's 22 and 23 with gate IC21A. This circuit provides a pulse every 20 bits to the section of Sync Control Circuitry that confirms synchronization. It also provides a narrow pulse every 40 bits to the Out-of-Sync Detector. The purposes of both pulse types will be explained under sections describing their respective destinations.

4.3.18 Out-of-Sync Detector

The Out-of-Sync Detector is essentially an error counter which separates incoming data into 40-bit blocks and checks each block for a quantity of errors in excess of twelve. More than twelve errors indicates an out-of-sync condition.

The detection process is accomplished by counting logical-error pulses from the Error-Select circuit during the 40-bit interval allowed by the reset pulse from the Bit Counter. Counting takes place in IC24A. The gate of IC19C opens for a count of 12 or more to release an out-of-sync pulse to the Sync Control Circuit.

4.3.19 Sync Control

Sync Control circuitry performs the opening and closing of the Sequence Generator feedback loop, and it regulates operation of both the NO SYNC and LOST SYNC indicators on the front panel. Its primary components are IC's 18A and 18B which make up a 2-bit shift register for purposes of sync confirmation.

Both stages of the 2-bit register are set under any of the three following conditions:

1. Actuation of the RESET/RESYNC button on the front panel.
2. A pulse from the Out-of-Sync detector.
3. Detection of an error before the shift register can be cleared. The shift register has a logical zero input and is toggled by the 20-bit output of the Bit Counter. There must therefore be two consecutive error-free blocks of twenty bits before the register is cleared.

- - -

Four gates at the shift-register output control the NO SYNC indicator and status of the Sequence Generator loop. If the second stage of the shift register is set, the Receiver is out of sync and the NO SYNC indicator is energized. Also, with the MODE switch set to VIOLATIONS, the NO SYNC indicator is forced on regardless of sync status. One of the four gates controls the NO SYNC indicator, while the remaining three control status of the Loop Control circuit.

Of the three remaining gates, one allows the shift register to control status of the Sequence Generator's feedback loop only in the automatic sync mode, while another gate ORs the automatic sync control with the manual sync command from the RESET/RESYNC pushbutton. The final gate inhibits the Sequence Generator's feedback loop from being opened by any means when the test set is set to measure bipolar violations.

For Violation measurements the Sequence Generator is used as a time base only, and it need not be synchronized with the received data. This is achieved by the final gate and the self-start capability of the Generator.

Finally, one flip-flop and one gate control operation of the LOST SYNC indicator. The flip-flop is set by output of the gates, mentioned above, when sync has been regained, and it energizes the indicator. The flip-flop can be reset only by operating the RESET/RESYNC switch. The gate forces the indicator on when the test set is instructed, via the MODE switch, to measure Violations.

4.3.20 Count Interval Control

The Count Interval Control consists of two decade counters, IC's 27A and 28A, along with several gates, and the COUNT INTERVAL switch (front panel). The counters tally word-sync pulses and provide outputs at one, ten and one hundred word intervals. The appropriate output is selected via the COUNT INTERVAL switch position and selection gates, and it is provided to the Display/Count control circuit.

Since a word-sync pulse is generated once for each cycle of the test sequence, actual count intervals corresponding to those listed for the Count Interval switch are listed below. Each cycle of the test sequence contains

<u>Count Interval Switch Setting</u>	<u>Actual Count Interval</u>
10^6	1.048575×10^6
10^7	1.048575×10^7
10^8	1.048575×10^8

1,048,575 bits, as explained in Section 4.2.2 on the Sequence Generator. Thus, count intervals are actually based on this quantity.

The two decade counters of the Count Interval Control are reset by the main reset line derived from the Display/Count Control. This line also resets the Display Counter.

4.3.21 Display Interval Timer

Timing for each display interval is supplied by a unijunction-type timer with a logic level inhibit and a logic level output. Two transistors, Q2 and Q3, are connected as the programmable unijunction device. Q1 inhibits operation of the timer by shorting capacitor C14 during the count interval. Q4 serves as a logic level output buffer.

The display interval can be varied from approximately one to ten seconds by means of the Display Interval potentiometer on the front panel. Switching the Display Interval control to "Continuous" operation opens the timer's charging path.

4.3.22 Display/Count Control

Two flip-flop, IC's 20B and 29, with several gates regulate the gating of errors to the Counter and the resetting of all counters by synchronizing to the Word-Sync, End-of-Count, and End-of-Display signals. At the start of each count interval, the word-sync pulse forces flip-flop IC29, through inverter IC26, to drop the reset line and set count flip-flop IC20B. The count flip-flop, in turn, disables the Display Timer through Q1, opens error gate IC14, and turns on the front panel COUNT indicator. At the end of the count interval, the count flip-flop is reset, reversing the preceding step. The Display Timer then begins to time out unless the DISPLAY INTERVAL control is set on "HOLD".

At the end of time-out, flip-flop IC29 sets and causes all counters to reset to zero. They remain reset until the next word-sync pulse starts a new count cycle. Each count interval is synchronized to the Sequence Generator by the word-sync pulse, as described.

Operating the RESET/RESYNC button at any time produces the same result as the time-out pulse from the Display Timer.

4.3.23 Error Counter

The Error Counter is a two decade arrangement, IC's 1 thru 4. There is also an overflow flip-flop, IC29A. Both the counters and the overflow flip-flop are reset by the main reset signal from the Display/Count control.

4.3.24 Display

The Display consists of a two digit solid state affair with its decoder/drivers. The five front panel indicator lamps are also solid state. All light-emitting-diodes, seven segments for numerals and single segment for the indicators.

CHAPTER 5

MAINTENANCE

5.1 General

Routine care of the Test Set involves simply a periodic calibration. However, should a malfunction be suspected, a performance check is in order. And if a malfunction is definite, the Test Set must undergo troubleshooting procedure. This chapter presents separate sections on calibration, performance check, and troubleshooting. While the first two items are necessarily set procedures, the troubleshooting procedure is a suggested item and a guide. Whether or not the troubleshooting procedure is followed, the responsible technical authority is advised to read it through prior to commencing any investigation.

5.2 Test Equipment Requirements

- a. Frequency Counter: GR Model 1191 or equivalent
- b. Oscilloscope: Tektronix Model 547 or equivalent
- c. Oscilloscope Accessories: Tektronix Model 1A1 Plug-In or equivalent, with 2 each X10 Probes and 1 each X1 Probe (calibrate these items to be compatible with the Oscilloscope to be used).
- d. BNC to BNC Coaxial Cable
- e. Patch Cord with WE-310 type plug at each end
- f. Bell System J98710R T-1 Quasi Random Signal Source
- g. Tapped Termination, 1 each, per Figure 1
- h. Cable Simulator, 1 each, per Figure 2
- i. 24 dB Attenuator, 1 each, per Figure 3
- j. Termination, 3 each, per Figure 4
- k. Test Transmitter: Bowmar/ALI No. D271-129 or equiv.
- l. Test Receiver: Bowmar/ALI No. D271-130 or equiv.
- m. Resistor, 100 Ω , 1% with an alligator clip at each end.
- n. **Standard Error Rate Test Set.** This set must first have been qualified for use as an operating standard by (1) successfully passing Self Test requirements of Section 3.2 of the Technical Manual for the Error Rate Test Set, and (2) be certified as having synchronized to a Bell System J98710R T-1 Quasi Random Signal Source without recording errors (3) be certified to insert and detect both errors and violations exclusive of one another.

- o. Storage Oscilloscope: Tektronix Model 549 or equivalent (see above for accessories).
- p. D.C. Power Supply: Power Designs Model TW5005 or equivalent.

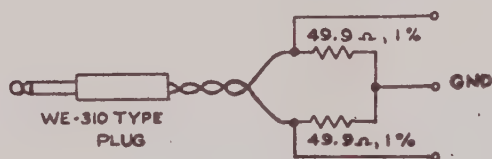


Figure 1: Tapped Termination (1 required)

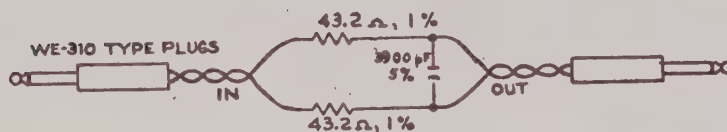


Figure 2: Cable Simulator (1 required)

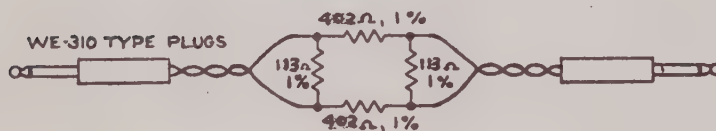


Figure 3: 24 dB Attenuator (1 required)



Figure 4: Termination (3 required)

5.3 Calibration Procedure

5.3.1 Preliminary

- a. Remove the test set from its outer case.

CAUTION: Voltages as high as 115 Vac are present in the vicinity of the Power Switch and the Fuseholder.

- b. Apply 115 Vac power to the test set and turn on the Power Switch.
- c. Do not connect equipment to the test set except as directed below.

5.3.2 Oscillator Frequency Adjustment

(To be made only after a one-hour minimum warm-up.)

- a. Connect the Frequency Counter to the TRANSMIT BIT SYNC and GRD terminals on the front panel of the test set.
- b. Adjust the Frequency Counter for a one-second count.
- c. Adjust capacitor C3, at the rear edge of the Transmitter circuit board (A3) for a frequency of 1,544,000 Hz $\pm$ 5 Hz.

NOTE: On earlier revisions of the Transmitter circuit board (PM271-403/A and PM271-403/B), potentiometer R2 was used for the frequency adjustment. Refer to Section 6, Dwgs No. D271-103/C and D271-203/0.

- d. Disconnect the Counter.

5.3.3 Transmitter Amplitude Adjustment

- a. Properly calibrate the Oscilloscope, Plug-In, and X10 Probe with respect to both frequency and amplitude using the internal calibration source.
- b. Plug the test termination shown in Figure 1 into one of the four output jacks of the Test Set.
- c. Connect an X10 Oscilloscope probe between the GRD terminal and either one of the remaining terminals of the Tapped Termination (Figure 1).
- d. Set the Oscilloscope sweep for 0.1 μ sec/cm and vertical sensitivity for 0.05V/cm. Adjust potentiometer R6 (+5V Adjust), on the upper edge of the Power Supply board, for a pulse height of 1.5V (3 cm) peak or 3.0V (6 cm) peak-to-peak as shown in Figure 5.

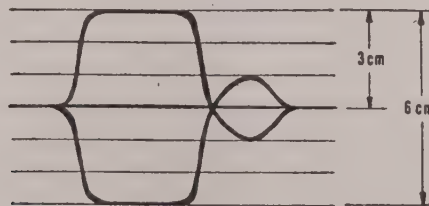


Figure 5: Transmitter Amplitude

- e. Disconnect the Oscilloscope Probe and unplug the test termination from the Transmitter output jack.

5.3.4 Clock Extractor Timing Adjustment

- a. Set up the Oscilloscope as follows:

Plug-In	MODE: CH 1
	INPUT SELECT: DC
	VOLTS/CM: 0.2V/CM

Time Base A

Mode:	Trig
SLOPE:	-
COUPLING:	AC LF Rej
SOURCE:	EXT.
TIME/CM:	0.1 μ s/cm
Horizontal Display:	A
Sweep Magnifier:	X1 OFF

- b. Using the X1 Probe, connect the TRANSMIT BIT SYNC, on the front panel of the test set to the EXTERNAL SYNC input of the Oscilloscope. Connect the Probe's ground lead to the GRD jack on the front panel of the test set.
- c. Using the X10 Probe, connect TP2 on the Receiver circuit board (center board) of the test set to the CH1 input of the Oscilloscope Plug-In. Connect the ground lead of the Probe to the edge foil of the circuit board.
- d. Remove the Receiver Logic board (outer left of set) from the test set to gain access to the L1 adjustment.
- e. Use a tuning tool to adjust inductor L1 on the Receiver board for a symmetrical square wave with clean transitions.
- f. Switch the Sweep Magnifier to X10 and adjust the Oscilloscope's position controls to bring a transition into view (See Figure 6).



Figure 6: Transition Adjustment

- g. Continue to adjust L1 for minimum spread on the transition edge, using the Oscilloscope's position controls to keep the pattern centered or conveniently located.
- h. Remove the Oscilloscope probes from the test set, and replace the Receiver logic board.

5.3.5 Clock Extractor Phase Adjustment

- a. Set up the Oscilloscope as follows:

Plug-In	MODE:	ALT
	INPUT SELECT:	DC
	VOLTS/CM:	0.2V/CM
Time Base A	MODE:	TRIG
	SLOPE:	-
	COUPLING:	AC LF REJ.
	SOURCE:	EXT.
	TIME/CM:	0.1 μ s/cm
	Horizontal	
	Display:	A
	Sweep Magnifier:	X5

- b. Connect a coaxial cable with BNC connectors between the TRIGGER OUT jack of the Plug-In to the EXT input of TIME BASE A.
- c. Using two calibrated X10 Probes, connect CH1 of the Plug-In to TP3 and CH2 to TP2, both on the Receiver circuit board (center board) of the test set.
- d. Adjust the position controls and the TIME/CM vernier of the Oscilloscope to obtain the pattern of Figure 7, with the upper trace symmetrically positioned.

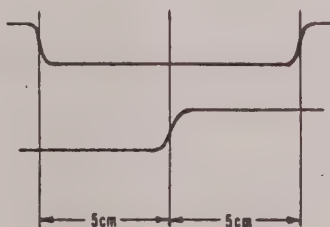


Figure 7: Clock Extractor Phase Adjustment

- e. Adjust capacitor C11, on the Receiver board (center), to position the lower trace at the center of the upper trace.

NOTE: On earlier revisions of the Receiver circuit board (PM271-402/A through PM271-402/D, potentiometer R22 was used for the phase adjustment. It may not be possible to exactly center the transition using R22; in which case, the transition should be brought as close to its proper position as possible. Refer to Section 6, Dwgs No. 271-102/F and D271-202/0.

- f. Disconnect the Oscilloscope from the test set.

5.3.6 No Data Threshold Adjustment

(Not applicable to earlier revisions PM271-402/A through PM271-402/D.)
(Not applicable to -212 Receiver Board)

- a. Push and hold the SELF TEST switch to INTERRUPT DATA and observe the NO DATA indicator.
- b. If the NO DATA indicator is on, adjust potentiometer R52, on the Receiver Module (A4), counterclockwise until the NO DATA indicator goes off. If the indicator is off, proceed with the next step.
- c. Slowly adjust the potentiometer clockwise until the NO DATA indicator turns on. Continue adjusting the potentiometer three (3) full turns past this point.
- d. Check the operation of the NO DATA indicator as the SELF TEST switch is operated to its INTERRUPT DATA position and released to NORMAL.

5.3.7 Final

- a. Return the test set to its case and secure with the four rear screws.
- b. Perform the Self Test (Chapter 3) as a final check of the instrument.

5.4 Performance Checks

5.4.1 Preliminary

These checks are to be made with the Test Set in its case. They may serve for periodic maintenance, quality control checks, and for post-repair checkout. The Error Rate Test Set must be connected to a power source of 115 VAC $\pm 10\%$, 50 to 60 Hz.

5.4.2 Transmitter Checks

5.4.2.1 Transmitter Clock Frequency

- a. Allow the Test Set to temperature stabilize by operating for at least one hour at room temperature. The Test Set may be momentarily unplugged only for the purpose of moving it.
- b. Connect the Counter input to the TRANSMITTER BIT SYNC pm jack and the GRD terminal located in the lower left section of the front panel.
- c. Adjust the Counter for a one-second count interval (to read directly in Hz), and set the Counter's input controls for a consistent display. The Counter should register between 1,543,950 and 1,544,050 at the end of each count interval.
- d. Disconnect the Counter.

5.4.2.2 Bipolar Output

- a. Check calibration of the Oscilloscope and a X10 probe with respect to frequency compensation and gain, using the internal calibration source of the Oscilloscope and the Oscilloscope manufacturer's procedure.

- b. Connect the cord of the test circuit shown in Figure 1 to one of the DS-1 Output jacks of the Test Set, and insert the three Terminations (Figure 4) into the remaining output jacks. Attach the GRD lead of the X10 probe to the GRD, center, tap of the test circuit and the probe tip to either of the outer taps.
- c. Adjust the Oscilloscope for a vertical sensitivity of 0.05V/division and a sweep-rate of 0.1 μ sec/division (magnifier off). Adjust the trigger, intensity, and position controls to obtain the waveform shown in Figure 8.
- d. The measurements designated (1) and (2) in Figure 8 should be between 2.7 and 3.3 cm (1.35 and 1.65 volts). Measurements (1) and (2) should differ by not more than 0.15 cm (0.075 volts).
- e. Measurements (3) and (4) should be between 3.0 and 3.5 cm (300 and 350 nsec). Measurements (3) and (4) should differ by not more than 0.15 cm (15 nsec).
- f. Measurements (5) and (6), taken between 10% and 90% of peak points, should be less than 0.8 cm (80 nsec).
- g. Measurement (7) should be between 10% and 30% of the base line to peak reading (nominally 0.3 to 0.9 cm for a 3.0 cm peak).
- h. Measurement (8), taken 4.0 cm to the right of the point of measurement (7), should be less than 10% of measurement (7) (Note: It may be necessary to increase the vertical sensitivity in order to make this measurement.)

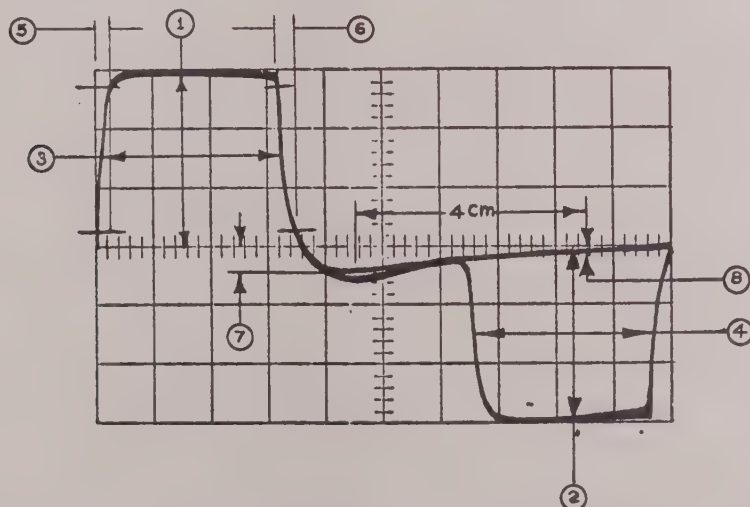


Figure 8: Bipolar Waveform

- i. Exchange output jack connections with the Tapped Termination and one of the three other Terminations. Repeat steps d thru h, above.

- j. Repeat step i, using a new output jack for the Tapped Termination.
- k. Repeat step j. The Tapped Termination should now have been used in all four output jacks.
- l. Remove the three terminations one at a time observing the Oscilloscope trace. The trace should not be altered as the terminations are removed. Finally, move the Tapped Termination to one of the three other output jacks. The waveform of Figure 8 should reappear on the Oscilloscope.
- m. With no connection to the DS-1 Input jack, momentarily operate the SELF TEST switch to both INTERRUPT DATA and INSERT ERRORS while observing the Oscilloscope.
- n. The Oscilloscope waveform should remain unchanged. Disconnect the Tapped Termination from the Test Set.

4. 2. 3 Pattern Content and Error Insertion

- a. Connect the Patch Cord between one of the Test Set's outputs and the input of the Standard Test Set (called out under Test Equipment Requirements).
- b. Set controls for the Standard Test Set as follows:

MODE:	ERRORS
SYNC MODE:	AUTO
DISPLAY INTERVAL:	1 Second
COUNT INTERVAL:	10 ⁶ Bits

- c. The NO DATA and NO SYNC indicators of the Standard Test Set should be off, and its Display should be reading a continuous '00'.
- d. Set the MODE switch of the Test Set under check to ERRORS and hold its SELF TEST switch at the INSERT ERRORS position. The Display of the Standard Test Set should count to a final reading of '08' at the end of each full count interval. (To the eye, the Display may appear to count by '02's)
- e. Set the MODE switch of the Test Set under check to VIOLATIONS and continue holding its SELF TEST switch at INSERT ERRORS. The Standard Test Set's Display should clear to, and remain at, '00'.
- f. Set the MODE switch of the Standard Test Set to VIOLATIONS and continue holding the SELF TEST switch of the Test Set under check at INSERT ERRORS. The Standard Test Set's Display should count to a final reading of '08' at the end of each full count interval. (To the eye, the display may appear to count by '02's)

- g. Set the MODE switch of the Test Set under check to ERRORS, and continue holding its SELF TEST switch at INSERT ERRORS. The Standard Test Set's Display should clear to '00'.
- h. Release the SELF TEST switch, and remove the Patch Cord connection.
- i. Set controls of the Storage Oscilloscope as follows:

Vertical V/cm:	0.1 V/cm
Upper Screen Storage:	Store
Lower Screen Storage:	Store
Screen Selector:	Full
Auto Erase:	Off
Time/cm A:	2 μ sec/cm
Horizontal Display:	A, Single Sweep
Magnifier:	Off
Triggering Mode:	Trig
Slope:	- (negative)
Coupling:	AC LF REJ
Source:	EXT.
- j. Connect a X1 probe to the Trigger input of the Storage oscilloscope. Insert the probe tip (preferably using a spring tip) into the TRANSMIT WORD SYNC jack of the Test Set. Attach the probe's ground lead to the GRD terminal on the front panel of the Test Set.
- k. Connect the two outputs of the D. C. Power Supply (s) at 5.7 ± 0.2 Vdc, to the Power Input jacks of the Test Receiver (see Test Equipment Requirements list, Section 1.0). Connect a Patch Cord between the Input jack of the Test Receiver and a DS-1 output of the Test Set.
- l. Connect a X10 Oscilloscope probe between the input of the Storage Oscilloscope and the Output and GRD terminals of the Test Receiver.
- m. Operate the Level and Stability controls and the Erase and Reset button of the Oscilloscope to obtain the waveform of Figure 9. The waveform should appear each time the pushbutton is operated. Observe the waveform carefully; it should contain fourteen time slots in which there are no pulses.

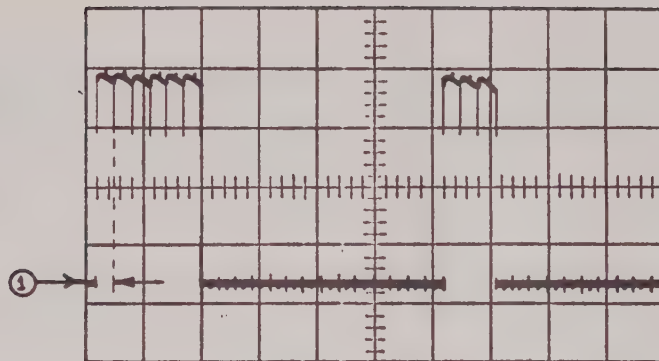


Figure 9: Typical 14-zero Condition
With No Errors

- n. Hold the Test Set's SELF TEST switch at INSERT ERRORS, with the MODE switch in its ERRORS position.
- o. While holding the SELF TEST switch, press and release the Oscilloscope's ERASE/RESET button. Again, carefully note the waveform. A pulse displayed earlier at the left of the screen should have disappeared, while another pulse has appeared such that there are now only thirteen time slots with no pulses. These conditions are shown in Figures 9 and 10. Also, measurement ①, as measured from the beginning of the trace, should be between 0.3 and 0.5 cm (600 and 1000 ns).

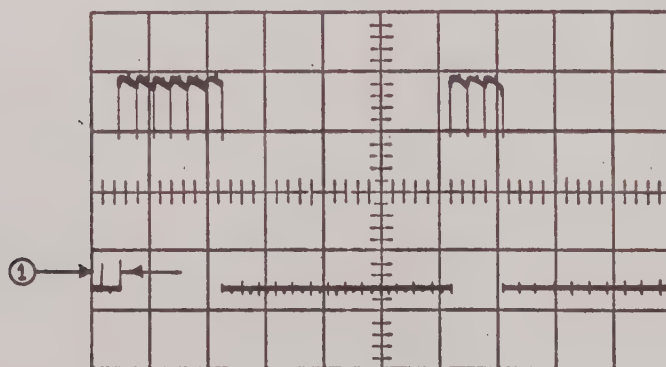


Figure 10: Typical 13-zero Condition
With two Errors

5.4.3 Receiver Checks

5.4.3.1 General Functional Check

- a. Perform the complete Self Test Procedure (see Section 4.0 of this procedure).

- b. Return all Test Set controls to the initial switch positions specified in Section 4.1, under Self Test Procedure.

5.4.3.2 Receiver Sensitivity to Level and Data Content

- a. Connect the input plug of the Cable Simulator (Figure 2) to one of the Test Set's DS-1 output jacks, while connecting the output plug to the Test Set's input jack. The NO DATA indicator should be off, and the Display should read '00' at all times.
- b. Remove the Cable Simulator, and insert the 24 dB Attenuator (Figure 3) in its place. The 24 dB Attenuator is a symmetrical circuit, so that it has no requirement for input and output designations for its plugs. The NO DATA indicator should be off, and the Display should read '00' at all times.
- c. Hold the Test Set's SELF TEST switch at its INTERRUPT DATA position. The NO DATA indicator should remain off.
- d. Release the SELF TEST switch and remove the 24 dB Attenuator. Connect the two outputs of the DC Power Supply, set for 5.7 ± 0.2 Vdc, to the Power Input jacks of the Test Transmitter (see Test Equipment Requirements list, Section 1.0). Connect a 24dB Attenuator between the Output jack of the Test Transmitter and the DS-1 input jack of the Test Set.
- e. Set the Test Transmitter's rotary switch to its '16' position. In this position, the Test Transmitter provides a bipolar pattern of a single '1' followed by fifteen '0's', provided its Reset button has not been actuated.
- f. Press and hold the Test Transmitter's Reset button. The NO DATA indicator, on the Test Set, should go on immediately (in less than 100 msec).
- g. Release the Reset button. The NO DATA indicator should go off and the Display read to '00' at all times.

For units with Serial Numbers greater than 630 perform the following steps h - m.

- h. Set the Test Transmitter's rotary switch to its '31' position. In this position, the Test Transmitter provides a bipolar pattern of a single '1' followed by thirty '0's, provided its Reset button has been pressed and released.
- i. Press and hold the Test Transmitter's Reset button. The NO DATA indicator, on the Test Set, should go on immediately (in less than 100 msec).
- j. Release the Reset button. The NO DATA indicator should go off.
- k. Set the Test Transmitter's rotary switch to its '50' position. In this position, the Test Transmitter provides a bipolar pattern of a single '1' followed by forty-nine '0's, provided its reset button has been pressed and released.
- l. Press and hold the Test Transmitter's Reset button. The NO DATA indicator on the Test Set should go on immediately (in less than 100 msec).
- m. Release the Reset button. The NO DATA indicator should remain on.

5.4.3.3 Auxiliary Output Checks

- a. Remove any connection from the Test Set's DS-1 input jack, and set front panel controls as follows:

MODE:	ERRORS
SELF TEST:	NORMAL
SYNC MODE:	MANUAL
COUNT INT.:	CONT.

- b. Set the Oscilloscope controls as follows:

Vertical V/cm:	0.1 V/cm
Coupling (Voltage):	D. C.
Time Base:	0.1 μ sec/cm
Triggering Mode:	TRIG
Triggering Slope:	- (negative)
Coupling (Trigger):	AC LF REJ
Source:	NORM

- c. Connect the ground lead of a properly calibrated X10 probe to the Test Set's front panel GRD terminal, and connect the probe tip (using a spring tip) to the Test Set's TRANSMIT BIT SYNC jack.
- d. Adjust the Oscilloscope's trigger level and position controls for the waveform of Figure 11. Measurement ① should be between 4.5 and 5.5 cm (4.5 and 5.5 volts). Measurement ② should be between 3.0 and 3.5 cm (300 and 350 nsec). Measurements ③ and ④, taken at the 10% and 90% points, should be less than 0.5 cm (50 nsec).

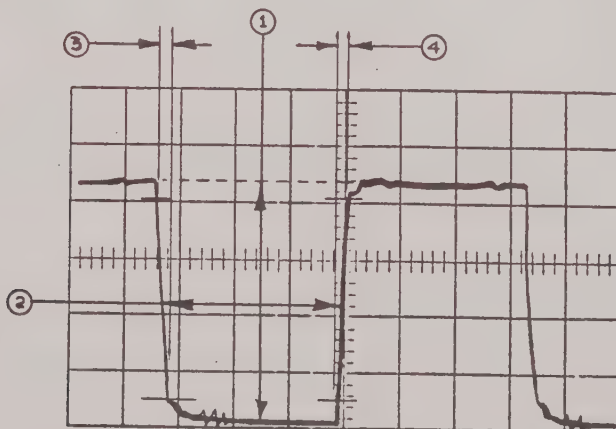


Figure 11: Transmit Bit Sync

- e. Using the 100 Ω , 1% Resistor whose ends are wired to alligator clips, fasten the Resistor between the probe's tip and the GRD terminal. Measurement ① of Figure 11 should now be not less than one half of Measurement ① taken in the previous step.

- f. Remove the probe tip and resistor from the TRANSMIT BIT SYNC jack. Insert the probe without Resistor into the RECEIVE BIT SYNC jack, and repeat steps d and e, above, using Figure 11 and the assigned measurement values.
- g. Remove the probe tip and resistor from the RECEIVE BIT SYNC jack. Insert the probe tip without resistor into the ERRORS jack. Momentarily push the SELF TEST switch to INTERRUPT DATA, to force the Receiver out of synchronization thereby producing a large number of errors.
- h. Observe the waveform of Figure 12. Measurement (1) should be between 4.5 and 5.5 cm (4.5 and 5.5 volts). Measurement (2) should be between 3.0 and 3.5 cm (300 and 350 nsec). Measurement (3) and (4), taken at the 10% and 90% points, should be less than 0.5 cm (50 nsec).

Using the 100 Ω , 1% resistor whose ends are wired to alligator clips, fasten the resistor between the probe's tip and the GRD terminal. Measurement (1) of Figure 12 should now be not less than one half of Measurement (1) taken in the previous step.

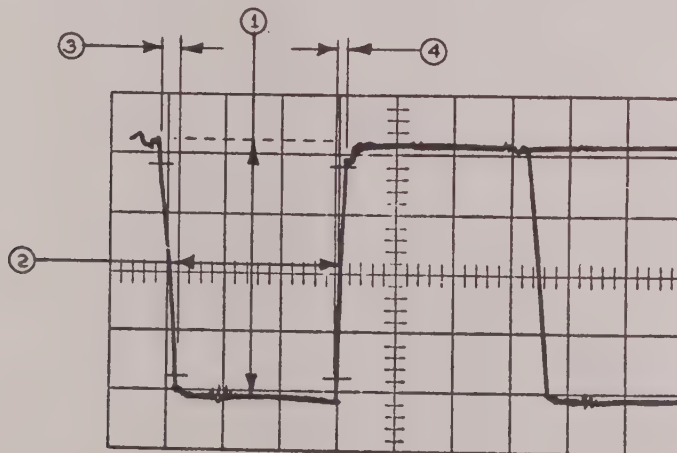


Figure 12: Errors

- i. Set controls of the Storage Oscilloscope as follows:

Vertical V/cm:	0.1V/cm
Upper Screen Storage:	Store
Lower Screen Storage:	Store
Screen Selector:	Full
Auto Erase:	Off

Time/cm A:	0.1 μ s/cm
Horizontal Display:	A, Single Sweep
Magnifier:	Off
Triggering Mode:	Trig
Slope:	- (negative)
Coupling:	AC LF REJ
Source:	NORM

- j. Using a properly calibrated X10 probe, connect the probe tip (preferably a spring tip) to the TRANSMIT WORD SYNC jack of the Test Set. Connect the probe's ground lead to the Test Set's GRD terminal.
- k. Operate the Storage Oscilloscope's Trigger, storage, and position controls to obtain the waveform of Figure 13, after the Erase & Reset button has been momentarily pushed. Measurement ① should be between 4.5 and 5.5 cm (4.5 and 5.5 volts). Measurement ② should be between 3.0 and 3.5 cm (300 and 350 nsec). Measurements ③ and ④, taken at the 10% and 90% points should be less than 0.5 cm (50 nsec).

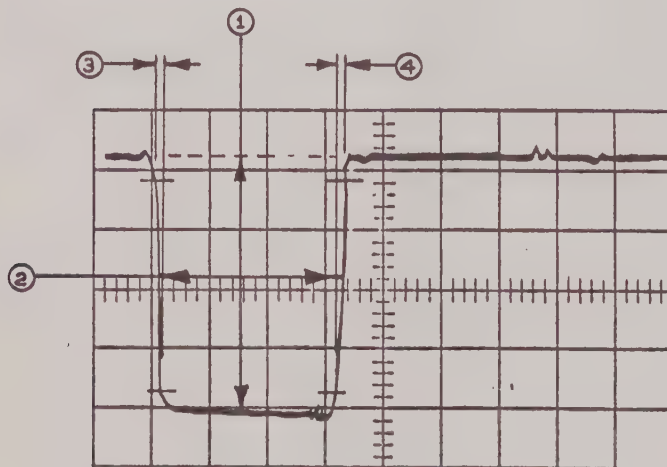


Figure 13: Transmit Word Sync

- l. Connect the alligator clip of the 100 Ω , 1% resistor between probe tip and ground connection. Measurement ①, from Figure 13, should be not less than 2.25 cm and 2.75 cm (2.25 and 2.75 volts).

- m. Remove the probe tip and resistor combination from the TRANSMIT WORD SYNC jack. Insert the probe tip only into the Test Set's RECEIVE WORD SYNC jack, and repeat steps k and l, above.
- n. Change the Storage Oscilloscope's triggering source control to EXT. Connect a X1 probe to the TRIG INPUT of the Oscilloscope. Connect the X1 probe's tip to the Test Set's TRANSMIT WORD SYNC jack and the probe's ground lead to the Test Set's GRD terminal. Connect the X10 probe between the Oscilloscope's vertical input and the Test Set's TRANSMIT BIT SYNC jack.
- o. Adjust the Oscilloscope's triggering controls to obtain the waveform of Figure 14. When properly triggered, the Oscilloscope should exhibit a slight delay (not more than 2/3 second) between release of its Erase & Reset button and the actual sweep. Measurement (1) should be between 1 and 3 cm (100 and 300 ns) from the beginning of the trace.

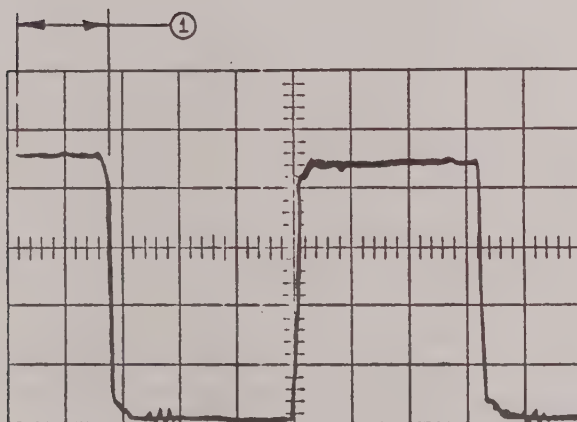


Figure 14: Transmit Bit Sync

5.5 Troubleshooting

5.5.1 Preliminary

Unless otherwise specified, the following procedures are to be performed with the Test Set in its case. Their intent is to aid in isolating the cause of malfunction to at least circuit board level.

In some cases, more than one procedure can be used to isolate a problem. The choice may be dictated by availability of test equipment.

Before proceeding, connect the Test Set to a power source of 115 Vac $\pm 10\%$, 50-60 Hz. The Test Set's fuse should have been checked and replaced if necessary.

CAUTION: If the Test Set is removed from its outer case, voltages as high as 115 Vac are present in the vicinity of the Power Switch and the Fuseholder.

Do not connect equipment to the Test Set except as directed below.

5.5.2 Power Supply Checks

- a. A Power Supply malfunction may be suspected if any of the following conditions exist.
 1. The Test Set repeatedly blows fuses of the proper size and type (Littlefuse 3AF Slo-Blo Fuse at 1/2 Amp).
 2. The Display and solid state indicators are too bright, too dark, or off (while Power indicator remains illuminated.)
 3. The Transmitter and Receiver simultaneously fail tests outlined in sections that follow.
- b. A suspected Power Supply malfunction can be confirmed by removing the Test Set from its outer case and checking the three test points visible through the opening in the right side plate. Voltages at the three test points should be as specified in the table below.

<u>Test Point</u>	<u>Voltage</u>
+5	+4.5 to +5.5 Vdc
-5	-4.5 to -5.5 Vdc
+5 ADJ	+4.0 to +6.0 Vdc

If a short circuit appears likely, remove the plug-in printed circuit boards one at a time while monitoring the shorted supply point. This action should narrow isolation of the short to one of the boards or to the chassis wiring.

NOTE: If the voltages measured above are not within specified limits, the plug-in boards should be removed from the Test Set until repairs are complete.

5.5.3 Transmitter Cross-Check

- a. Perform 5.4.2.3 a through h of the Performance Checks entitled Pattern Content and Error Insertion. Any failure indicated by these checks may be attributed to the Transmitter Board, printed circuit card A3.

- b. The Transmitter can be further analyzed by checking its bipolar output waveform against the Performance Checks of 5.4.2.2., entitled Bipolar Output.

5.5.4 Receiver Cross-Checks

NOTE: The receiver, error detectors and error counters are to be tested first as an entity although the circuits reside on three different printed circuit boards. Procedures for isolating the malfunction to any one board follow the overall receiver tests. Printed circuit board substitutions can also be used as an isolation technique if a replacement set of boards is available.

- a. Connect the Patch Cord between the input of the Test Set under check and one of the outputs of the Standard Test Set.
- b. Set the front panel controls of the two Test Sets as follows.

<u>Control</u>	<u>Test Set Under Check</u>	<u>Std. Test Set</u>
MODE:	VIOLATIONS	VIOLATIONS
SELF TEST:	NORMAL	NORMAL
SYNC MODE:	MANUAL	AUTO
COUNT INTERVAL:	10 ⁶	10 ⁶
DISPLAY INT:	FULL CCW (1 sec)	FULL CCW (1 sec)

- c. On the Test Set under check the indicators should respond as follows.

NO DATA:	OFF
NO SYNC:	ON
LOST SYNC:	ON
Numerical Display:	'00' at all times
OVERFLOW:	OFF
COUNT:	On for approximately 2/3 sec Off for approximately 3/4 to 1 1/2 sec

- d. If the Test Set under check operates in SELF TEST, i. e. with no input to the input jack, and not when connected to the Standard Test Set or vice versa, the malfunction may be located in the Receiver board, A2, in the connection between the input jack and the A2 board or in the SELF TEST switch.

- e. If the NO DATA indicator remains on and the COUNT indicator remains either on or off while signal is being supplied to the input jack, the malfunction is most likely in either the Receiver Module, A2, or the connection between this module and input jack.
- f. If the COUNT indicator remains off, momentarily depress the RESET/RESYNC button of the Test Set under check. If the COUNT indicator comes on within 2/3 sec. of the release of this button and remains on for 2/3 sec., the malfunction is most likely in either the DISPLAY INTERVAL control, the connections between the control and the RECEIVER LOGIC board, A1, or the discrete circuitry located on the front end of the A1 card.
- g. If the COUNT indicator remains on, momentarily depress the RESET/RESYNC button of the Test Set under check. If the COUNT indicator goes off when the button is depressed and comes on within 2/3 second of the button's release, the malfunction is most likely in either the COUNT INTERVAL control, the RECEIVER LOGIC board, A1, or the connections between the two.
- h. Assuming that the NO DATA indicator is off and the COUNT INDICATOR operates as described above, push and hold the SELF TEST switch of the Standard Test Set to its INSERT ERRORS position. The indicated count on the Display of the Test Set under check should clear to a starting count of '00' and progress to a final count of '08' while the COUNT indicator is on. During the counting process, the spacing of errors will cause the Display to appear to be counting by increments of '02'. At the count of '08', the Display should hold for the period set by the DISPLAY INTERVAL control, then it should clear to '00' and begin a new cycle.
- i. If the Display of the Test Set under check appears to be counting correctly but that one or more segments are missing from the display, the malfunction is located on the front panel of the Test Set.
- j. Change the COUNT INTERVAL control of the Test Set under check from 10^6 to 10^7 , and continue holding the SELF TEST switch of the Standard Test Set at its INSERT ERRORS position. The indicated count, on the Display, should perform as it did in Step h above. However, the final count should now be '80'.

- k. Change the COUNT INTERVAL control of the Test Set under check from 10^7 to 10^8 , and continue holding the SELF TEST switch of the Standard Test Set at its INSERT ERRORS position. The Display should cycle through a complete count of 0 to 100, a total of eight times. Since the Display contains only two digits, a count of 100 will register as '00' with an OVERFLOW indication. Again, spacing of errors will make the Display appear to be counting by increments of '02'.

The OVERFLOW indicator should come on at the first count of 100. It will remain on after this point, through the remaining seven cycles of 0 to 100. This entire process takes about 70 seconds.

- l. Change the COUNT INTERVAL control of the Test Set under check from 10^8 to CONT. The Display and OVERFLOW indicator should behave as in the preceding step (k) except that the Display will continue to cycle through 0 to 100 as long as the count interval is set for continuous running. The Test Set should be checked in this mode for at least 70 seconds.
- m. While holding the SELF TEST switch of the Standard Test Set at its INSERT ERRORS position, momentarily press the RESET/RESYNC button. The Display, and the COUNT and OVERFLOW indicators of the Test Set under check should reset. A new count interval should begin within 2/3 second of release of the button.
- n. Release the SELF TEST switch of the Standard Test Set and return the COUNT INTERVAL switch of the Test Set under check to its 10^6 position.
- o. Set the MODE switch of the Test Set under check for ERRORS and momentarily press the RESET/RESYNC button. The Display indication should be '00' at all times, while the NO DATA, NO SYNC, and LOST SYNC indicators should be off.
- p. If the NO SYNC indicator does not go off, yet the Test Set detected and recorded violations, the malfunction is most likely located in the RECEIVER LOGIC printed circuit board, the ERRORS/VIOLATIONS switch or the connection between the two.

NOTE: The out-of-sync condition is indicated by both the NO SYNC indicator and the fact that the Display will show '88' with an OVERFLOW indication during the count interval and any number with OVERFLOW at the end of the count interval.

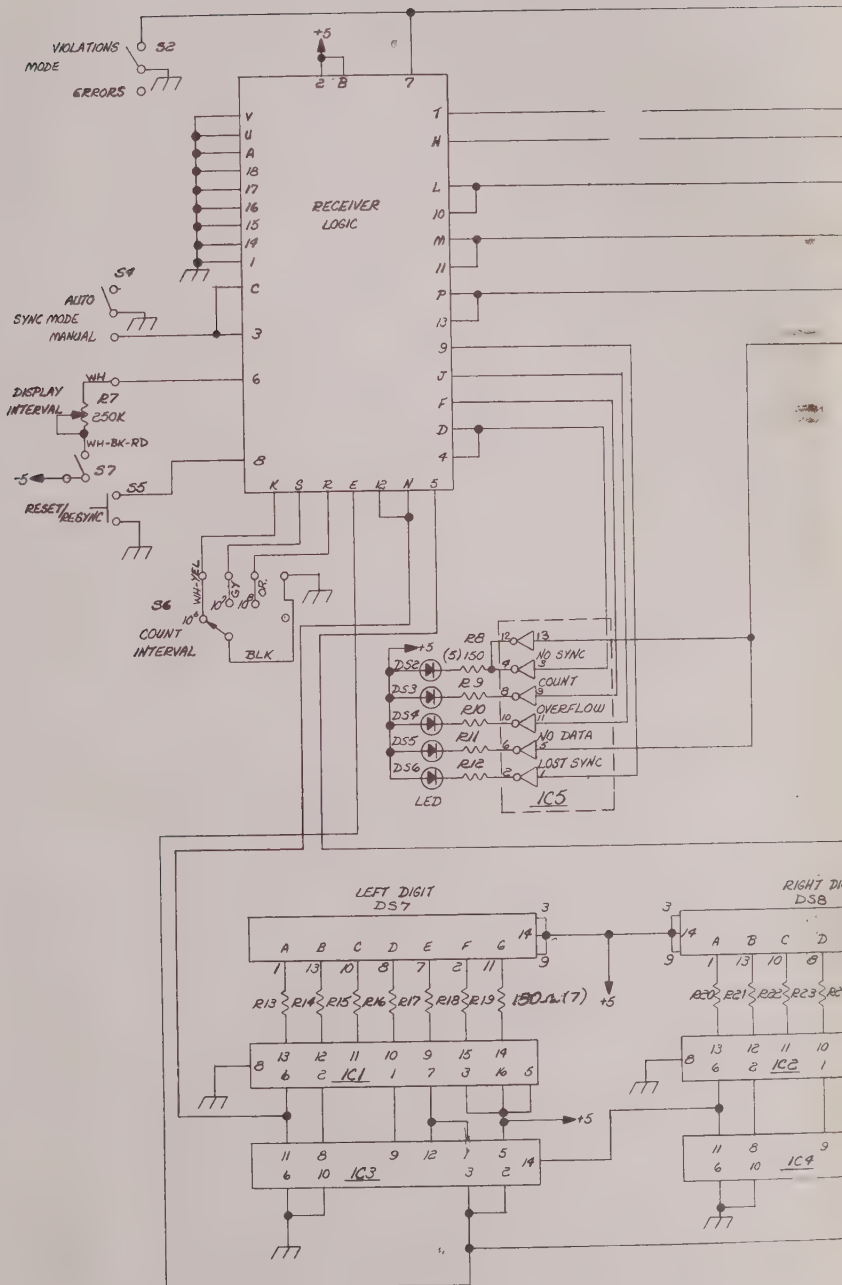
- q. Set the SYNC MODE switch of the Test Set under check to AUTO and remove the patch cord from the input jack of the Test Set under check. The NO DATA and NO SYNC indicators should come on immediately (in less than 100 ms). The LOST SYNC indicator may or may not come on.
- r. Reconnect the patch cord removed in the previous step. The NO DATA and NO SYNC indicators should go off. The LOST SYNC indicator should come on if not already on. The Display should show '00' errors.
- s. Momentarily pressing the RESET/RESYNC button should reset the LOST SYNC indicator and the NO SYNC indicator should remain off.
- t. Trouble completing the last three steps but not the earlier steps indicates that the malfunction is most likely in the RECEIVER LOGIC printed circuit board.

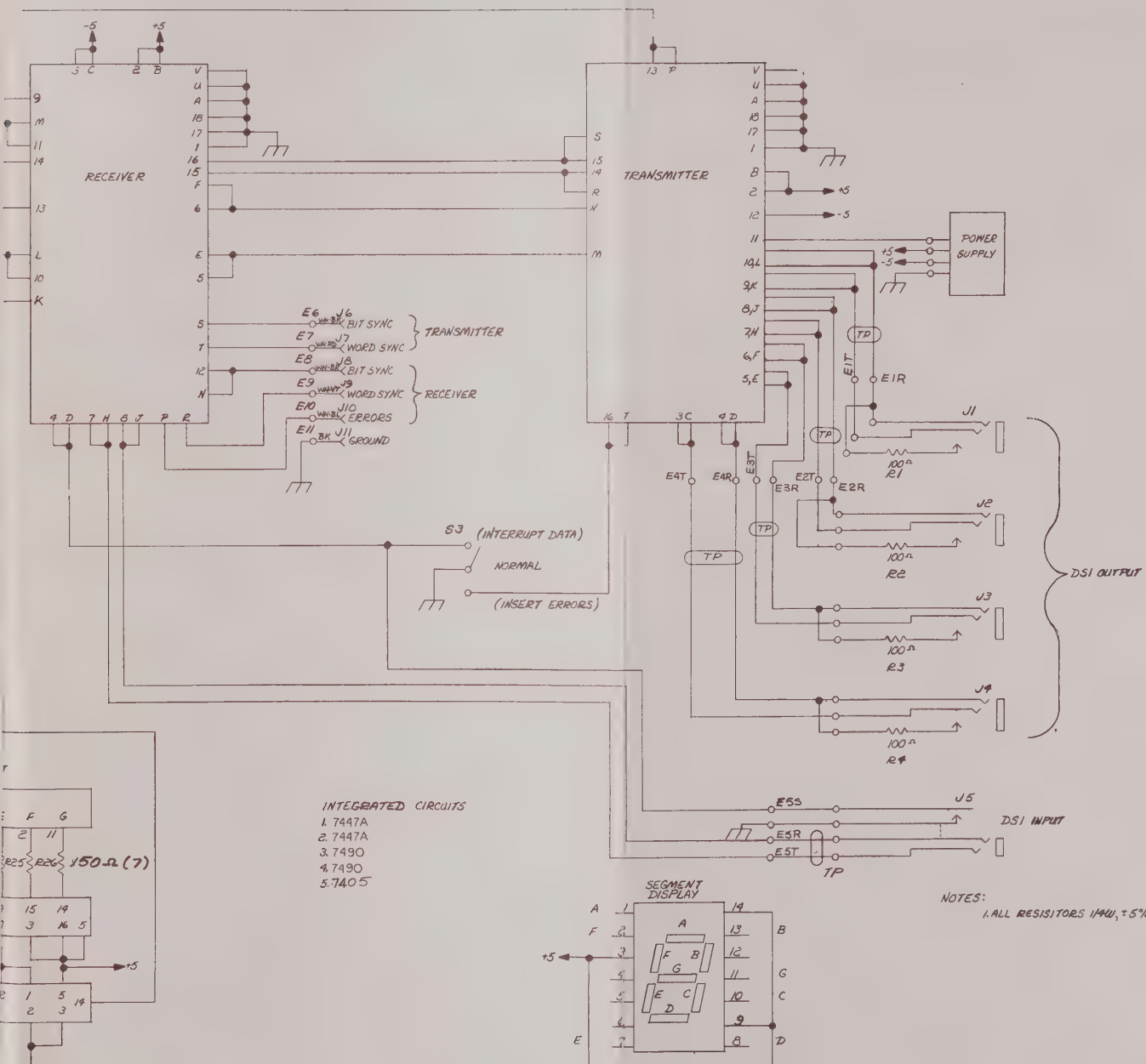
CHAPTER 6

DIAGRAMS

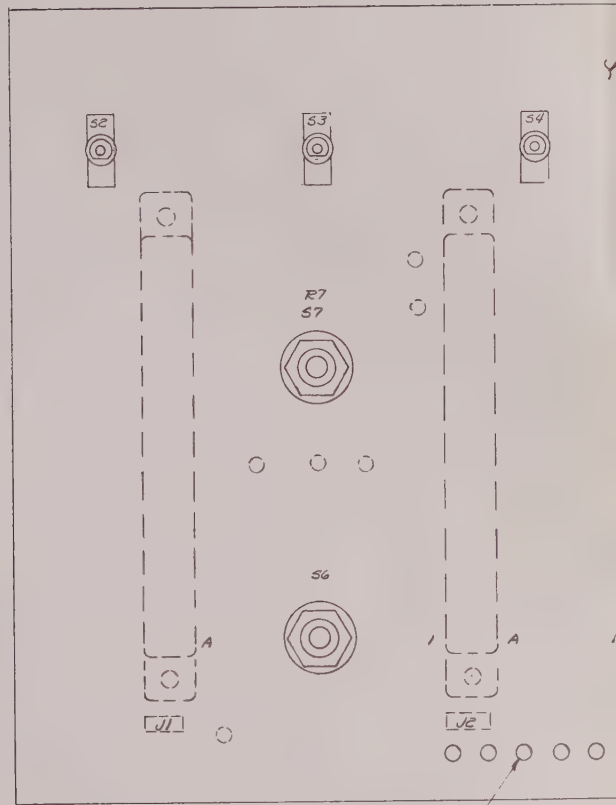
<u>Drawing Title</u>	<u>Drawing No.</u>
Front Panel Board Schematic	D271-100
Front Panel Board Assembly	D271-200
Receiver Logic Board Schematic	D271-101
Receiver Logic Board Assembly	D271-201
Receiver Board Schematic	D271-112
Receiver Board Assembly	D271-212
Transmitter Board Schematic	D271-103
Transmitter Board Assembly	D271-203
Power Supply Board Schematic	D271-104
Power Supply Board Assembly	C271-204
Main Assembly	E271-001
Receiver Board Schematic	* D271-102/F; D271-102
Receiver Board Assembly	* D271-202/0; D271-202
Transmitter Board Schematic	* D271-103/C
Transmitter Board Assembly	* D271-203/0

* These drawings reflect earlier revisions of these printed circuit modules and are included for reference purposes only.



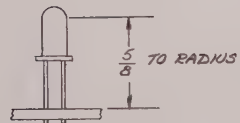


Front Panel Board Schematic
D271-100

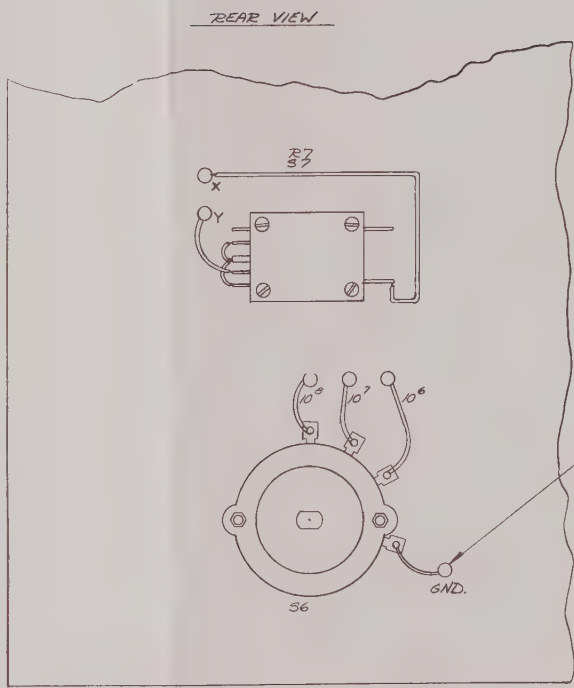
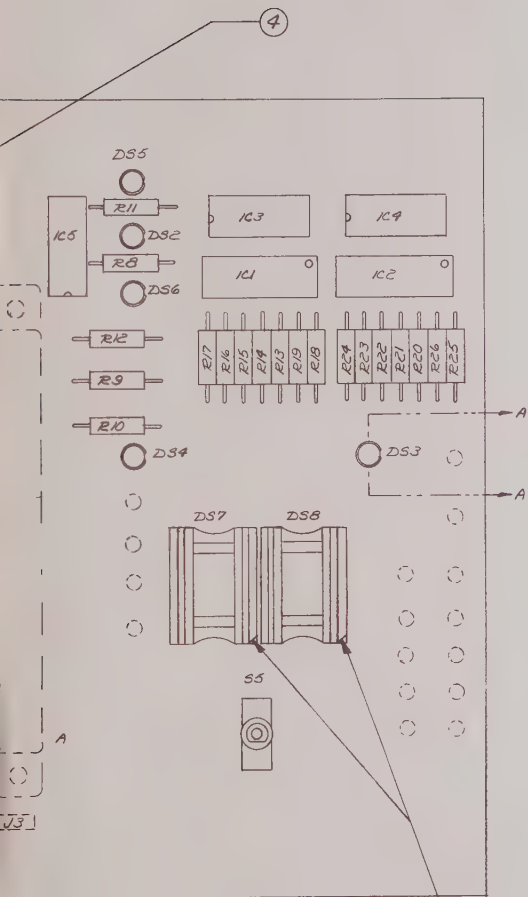


24 — EG THRUH MOUNT
TERMINALS THUS SIDE

NOTES 1. FOR LIST
2. FOR SC

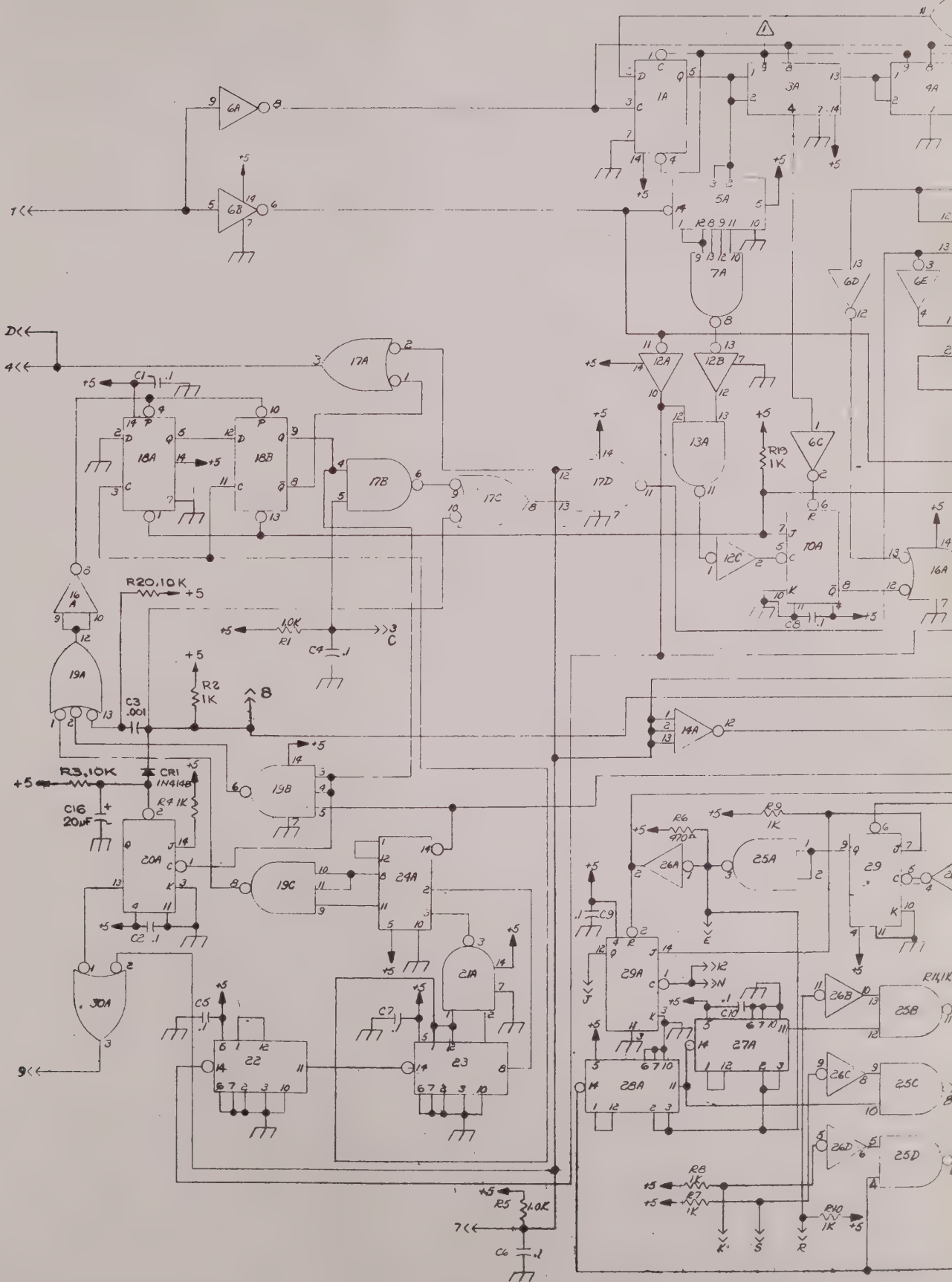


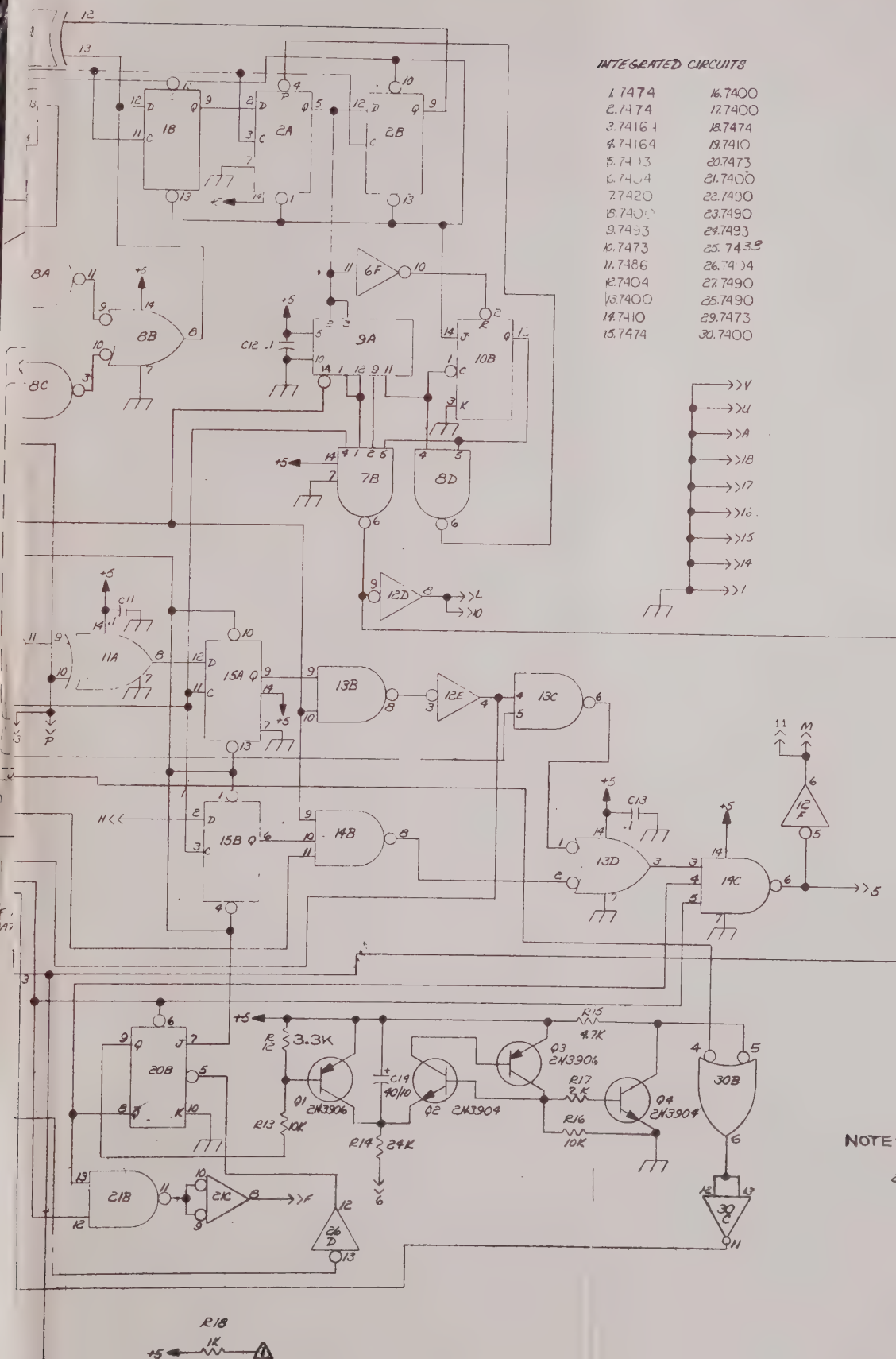
VIEW AT A-A
MOUNT D52, 3, 4, 5, 6 AS SHOWN



F MATLS SEE LM271-200
 ATIC SEE D271-100

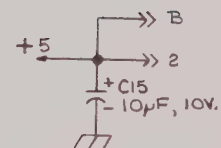
NOTE ORIENTATION
 OF SOCKETS



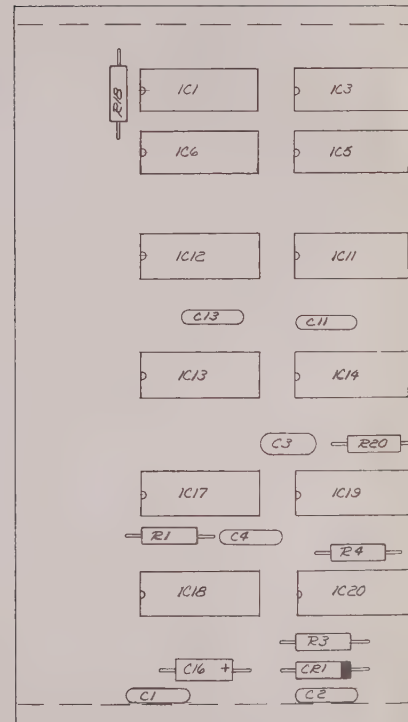


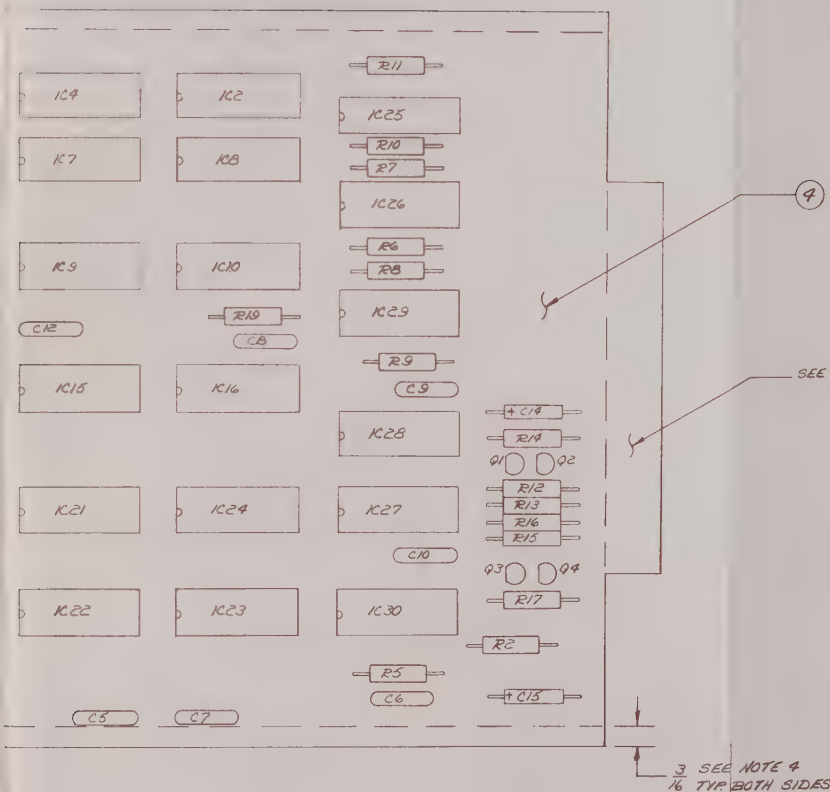
INTEGRATED CIRCUITS

1. 7474	16. 7400
2. 7474	17. 7400
3. 7416	18. 7474
4. 74164	19. 7410
5. 7413	20. 7473
6. 7404	21. 7400
7. 7420	22. 7400
8. 7401	23. 7490
9. 7493	24. 7493
10. 7473	25. 7432
11. 7486	26. 7404
12. 7404	27. 7490
13. 7400	28. 7490
14. 7410	29. 7473
15. 7474	30. 7400

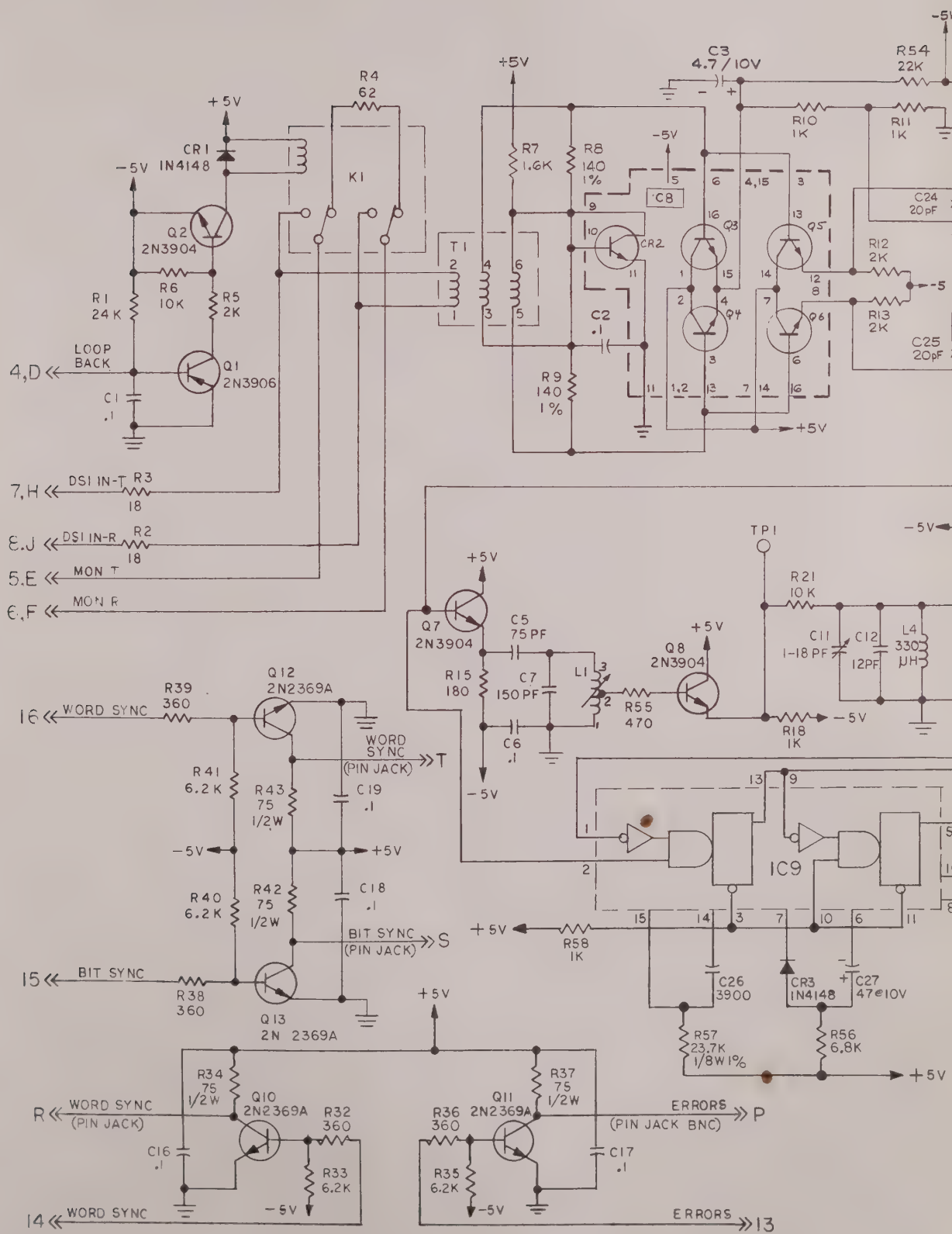


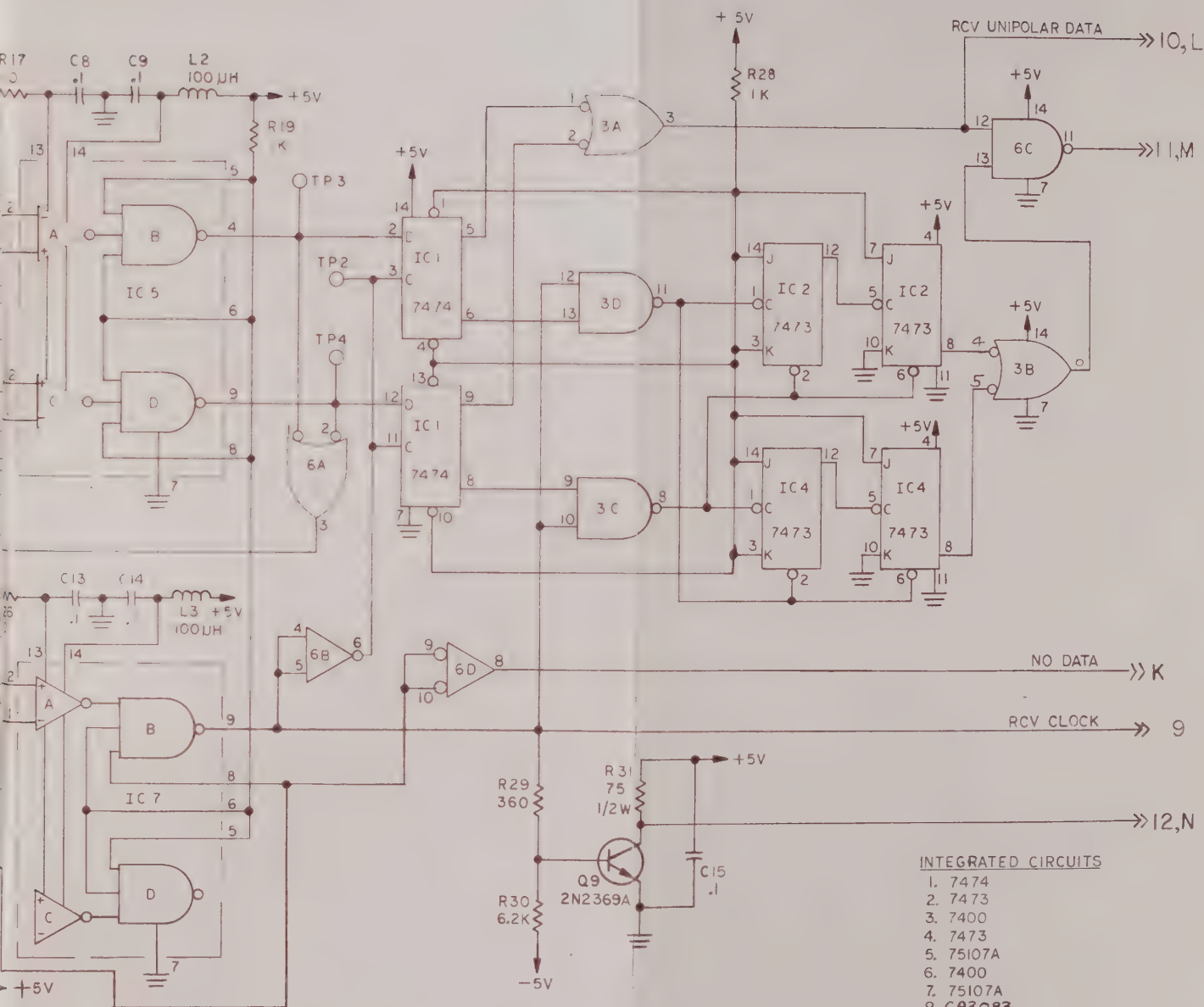
NOTE:
 1) ALL RESISTORS 1/4W, 5%
 2) ALL CAPS. IN MFD. UNLESS
 OTHERWISE NOTED.





- NOTES
1. FOR LIST OF MATERIALS SEE LM271-201
 2. FOR SCHEMATIC SEE D271-101
 3. COAT BOTH SIDES OF ASSEMBLY WITH ACRYLIC LACQUER #642 TYPE 3 PER WESTERN ELECTRIC WL-2243
 4. MASK (2) 3/16 STRIPS & CONTACT AREA, CIRCUIT & COMPONENT SIDES DURING COATING





INTEGRATED CIRCUITS

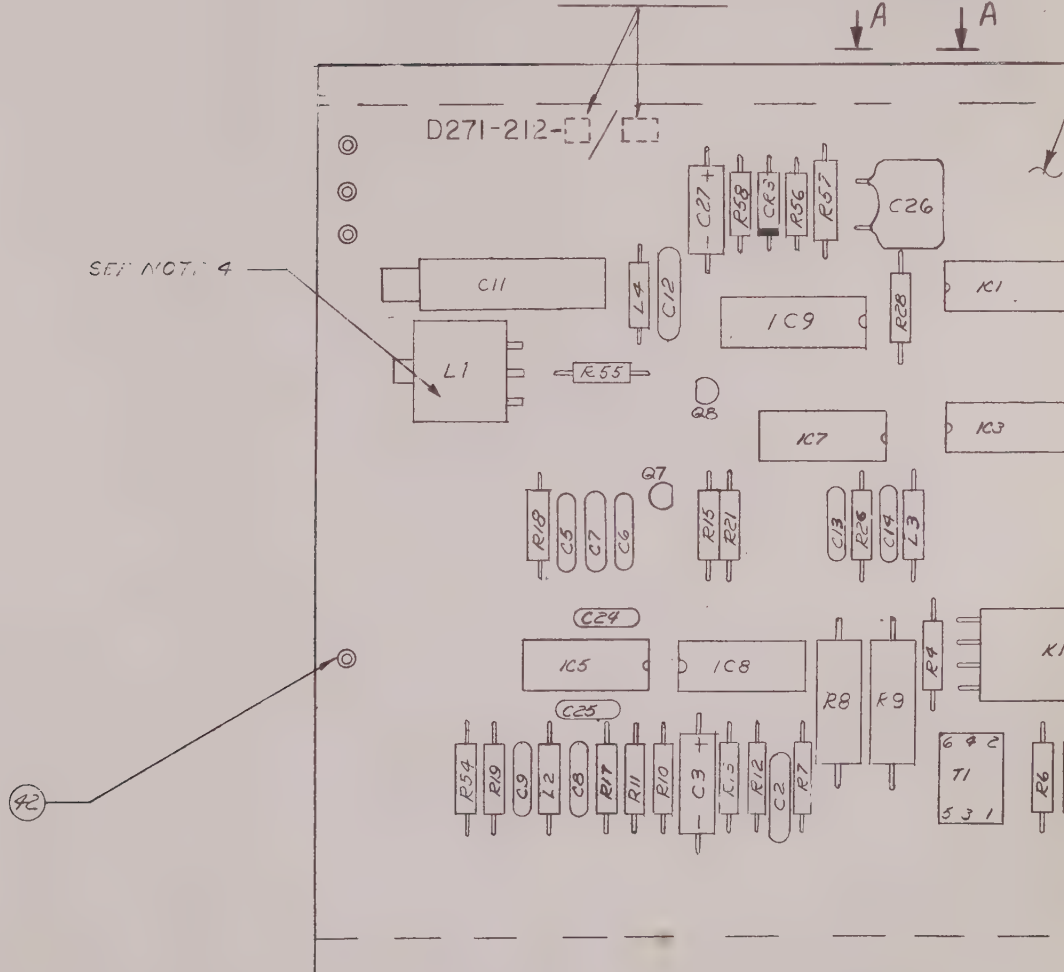
1. 7474
2. 7473
3. 7400
4. 7473
5. 75107A
6. 7400
7. 75107A
8. CA3083
9. 74123

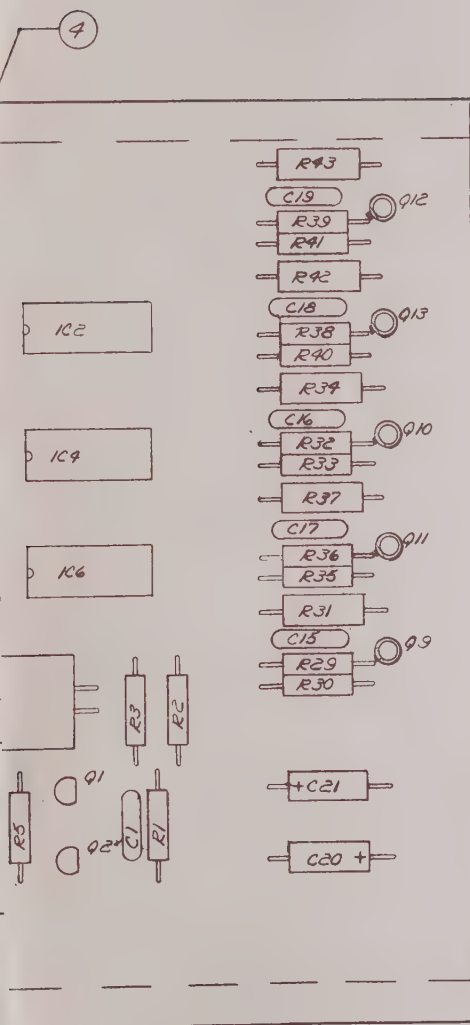
NOTES:

- UNLESS OTHERWISE NOTED —
1. ALL RESISTORS 5% 1/4 W. & IN OHMS
 2. ALL CAPACITORS ARE IN MICROFARADS.

DWG NO.	USED ON	
D271-212-1	271 C	A13
D271-212-2	271 A	A2

HANDSTAMP APPROPRIATE DASH NO. & REVISION
LETTER WITH WHITE EPOXY INK





SEE NOTE 4

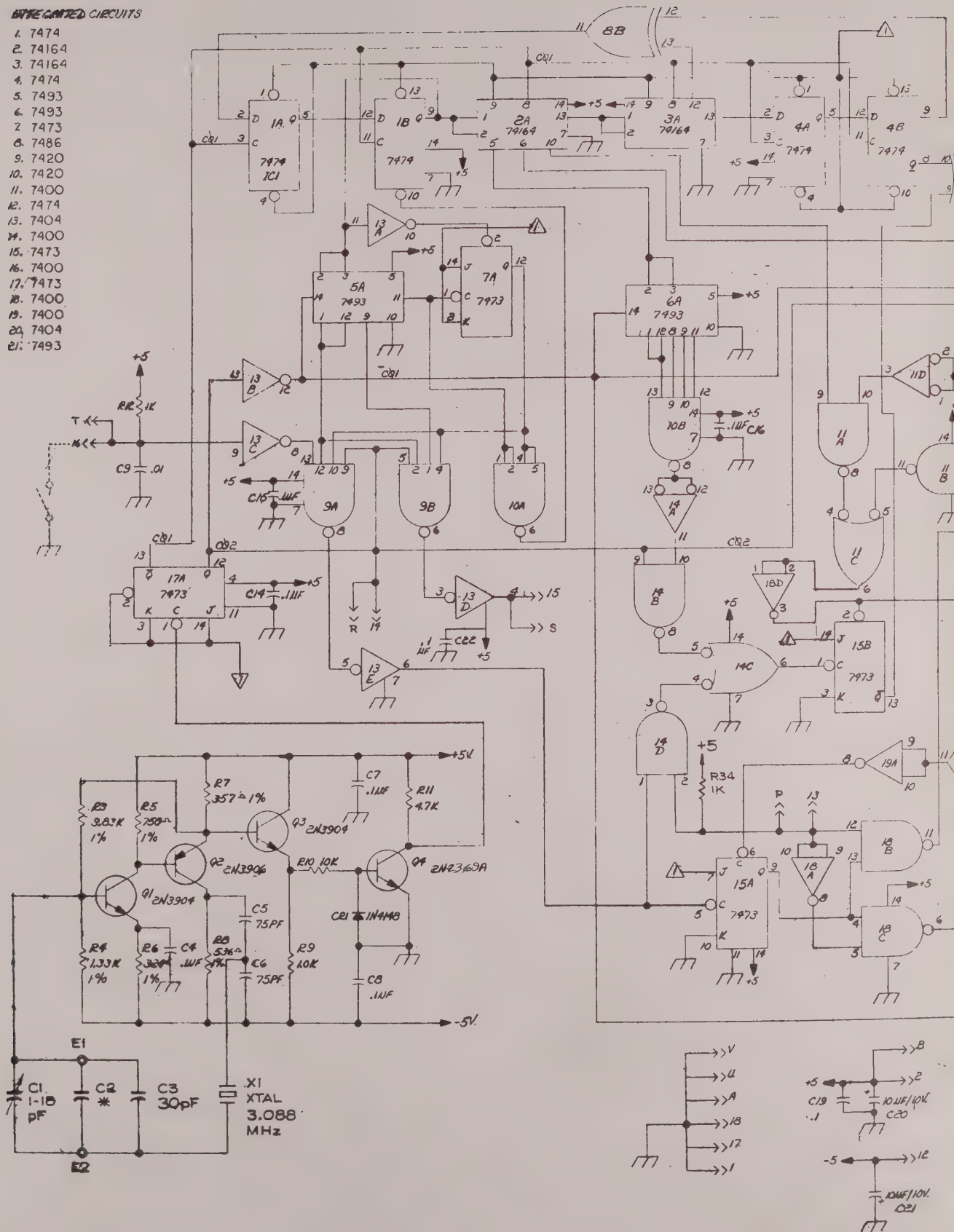
NOTES

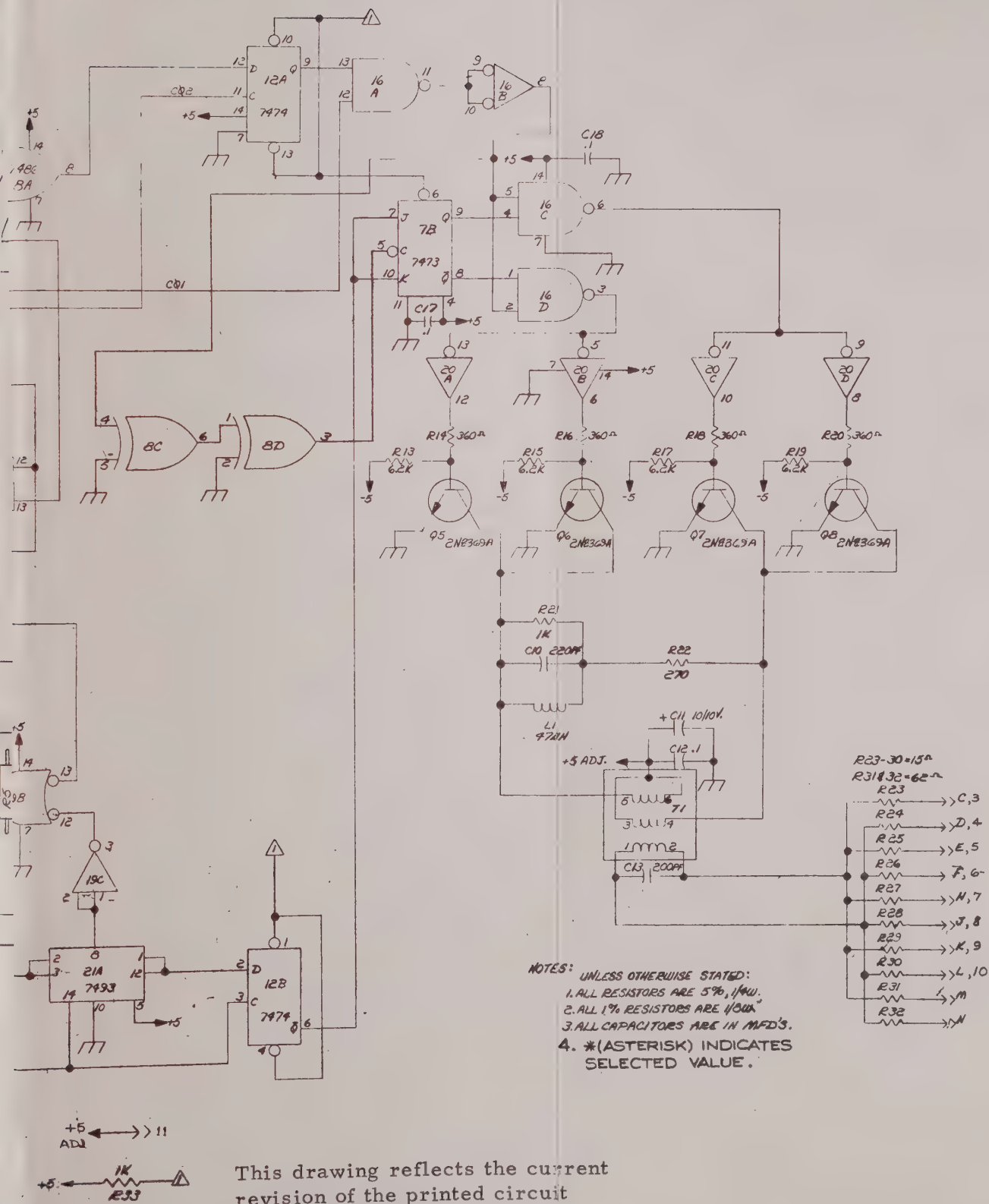
1. FOR LIST OF MAT'L'S SEE LM271-212
2. FOR SCHEMATIC SEE D271-112.
3. COAT BOTH SIDES OF ASSEMBLY WITH ACRYLIC LACQUER #692 TYPE 3 PER WESTERN ELECTEK WL-2293.
4. MASK (2) 3/16 STRIPS AND CONTACT AREA, CIRCUIT AND COMPONENT SIDES DURING COATING. ALSO MASK L1 & C11 ADJUSTMENT SCREWS, & ITEMS 42.

3 SEE NOTE 4
16 TYP. BOTH SIDES

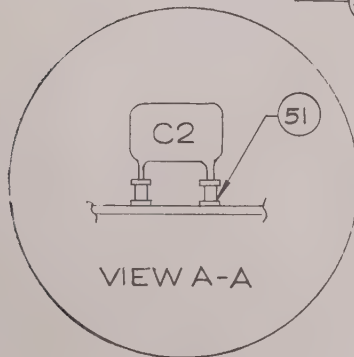
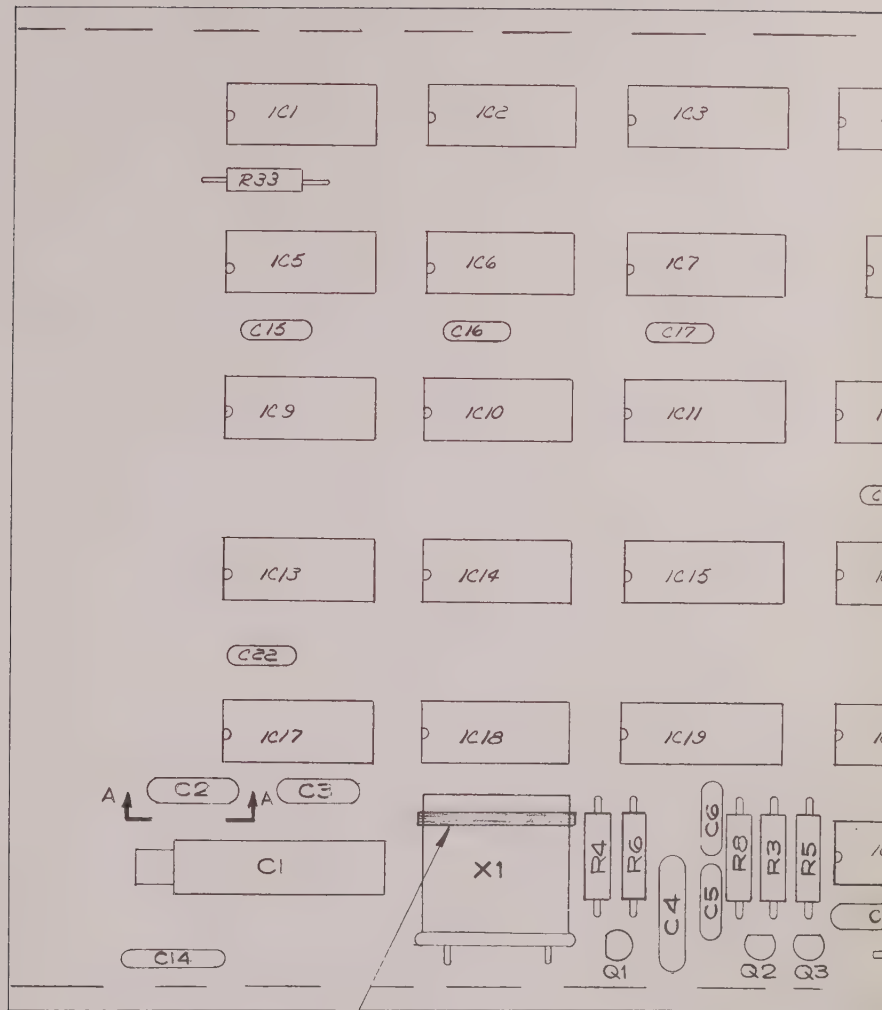
INTEGRATED CIRCUITS

1. 7474
2. 74164
3. 74164
4. 7474
5. 7493
6. 7493
7. 7473
8. 7486
9. 7420
10. 7420
11. 7400
12. 7474
13. 7404
14. 7400
15. 7473
16. 7400
17. 7473
18. 7400
19. 7400
20. 7404
21. 7493





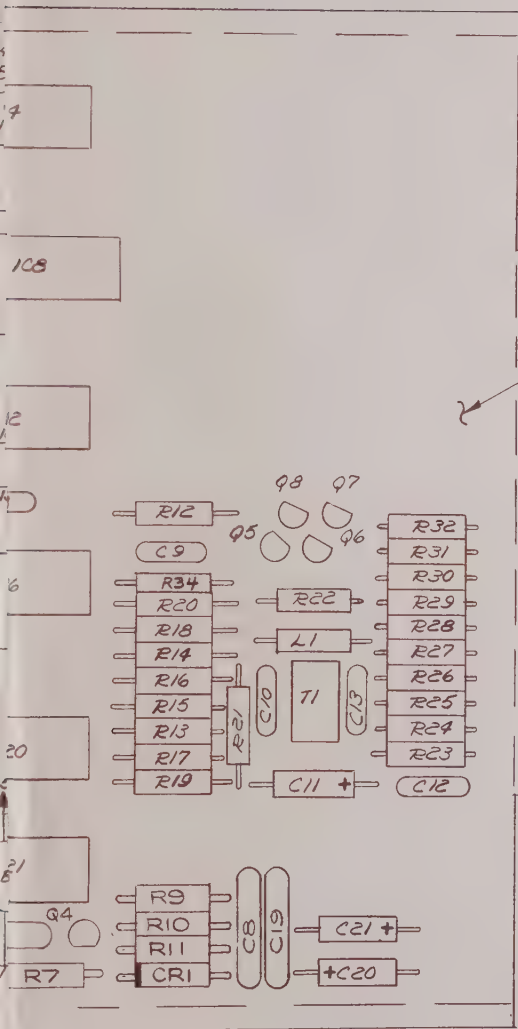
This drawing reflects the current revision of the printed circuit module; information reflecting an earlier revision may be found in the reference drawings at the end of this chapter.



50

51

VIEW A-A



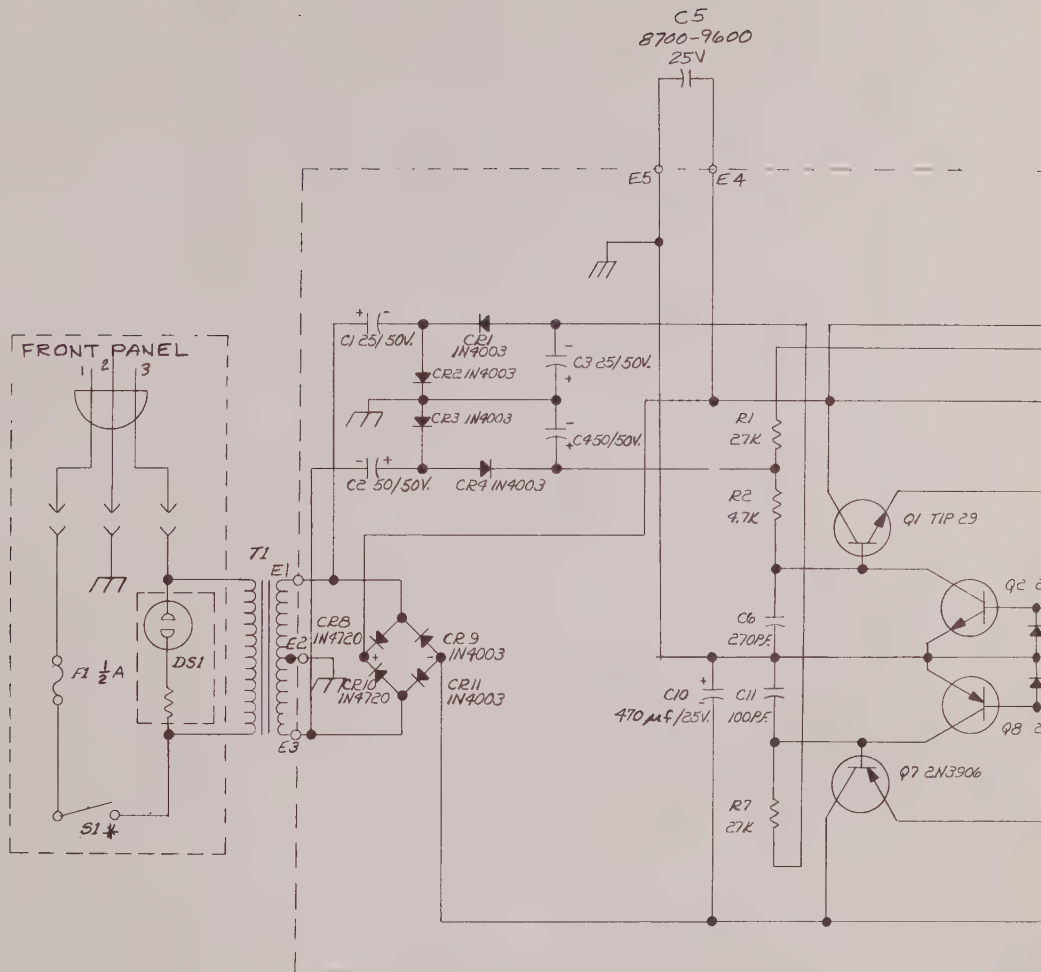
4

SEE NOTE
4.

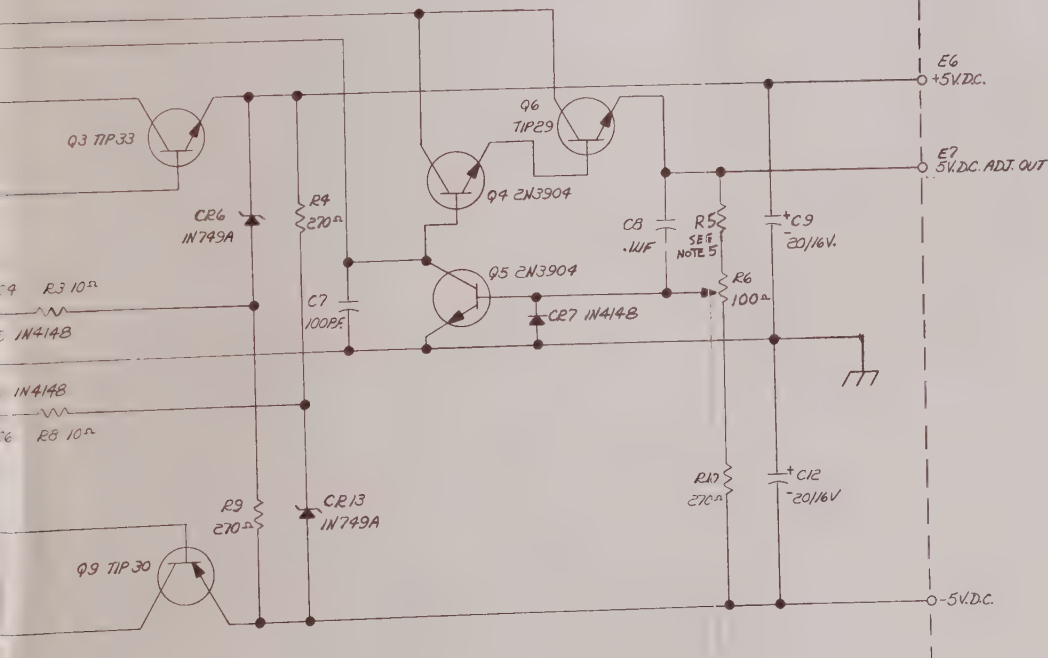
NOTES

1. FOR LIST OF MAT'L SEE LM271-203
2. FOR SCHEMATIC SEE D271-103.
3. COAT BOTH SIDES OF ASSEMBLY
WITH ACRYLIC LACQUER #642 TYPE 3
PER WESTERN ELECTRIC WL-2243.
4. MASK (2) 3/16 STRIPS & CONTACT
AREA, CIRCUIT AND COMPONENT SIDES
& C 1 DURING COATING.

3 SEE NOTE 4
16 TYP. BOTH SIDES.



POWER SUPPLY MODULE
ASSY C271-204



- NOTES: UNLESS SPECIFIED OTHERWISE
1. ALL RESISTORS 1/2W, 5%.
 2. ALL CAPS. ARE IN MFD'S.
 3. * ON 271B UNITS S1 CHANGES TO S5. ON 271C UNITS S1 CHANGES TO S11.
 4. POWER SUPPLY IS ASSEMBLY A4 ON 271A, AND ASSEMBLY A6 ON 271B AND C.
 5. "R5" IS A SELECT RESISTOR
220Ω FOR 271A & B UNITS (-2 SEQUENCE)
300Ω FOR 271C UNITS (-1 SEQUENCE)
SEE LM 271-204

5 MOUNT HEAT SINK TO
CIRCUIT BOARD AFTER
MASK THIS EDGE
DURING COATING

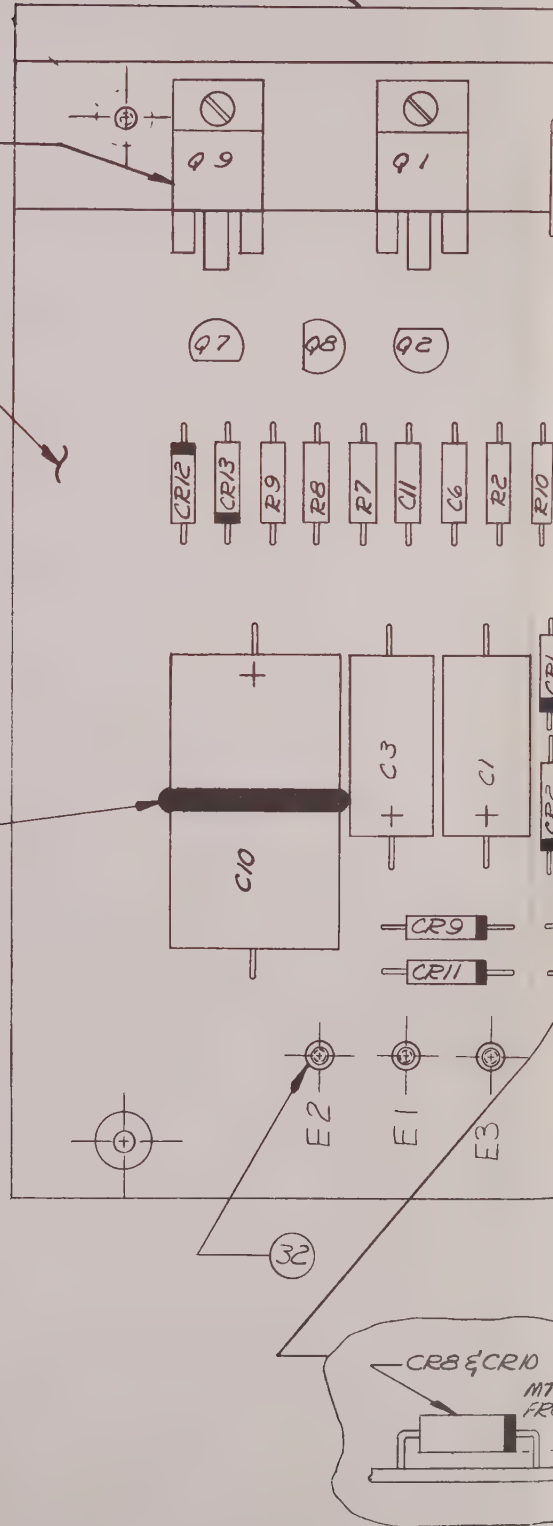
APPLY ITEM 33
TO BOTH SIDES OF MICA
INSULATOR, TYPICAL Q1, 3, 6, & 9

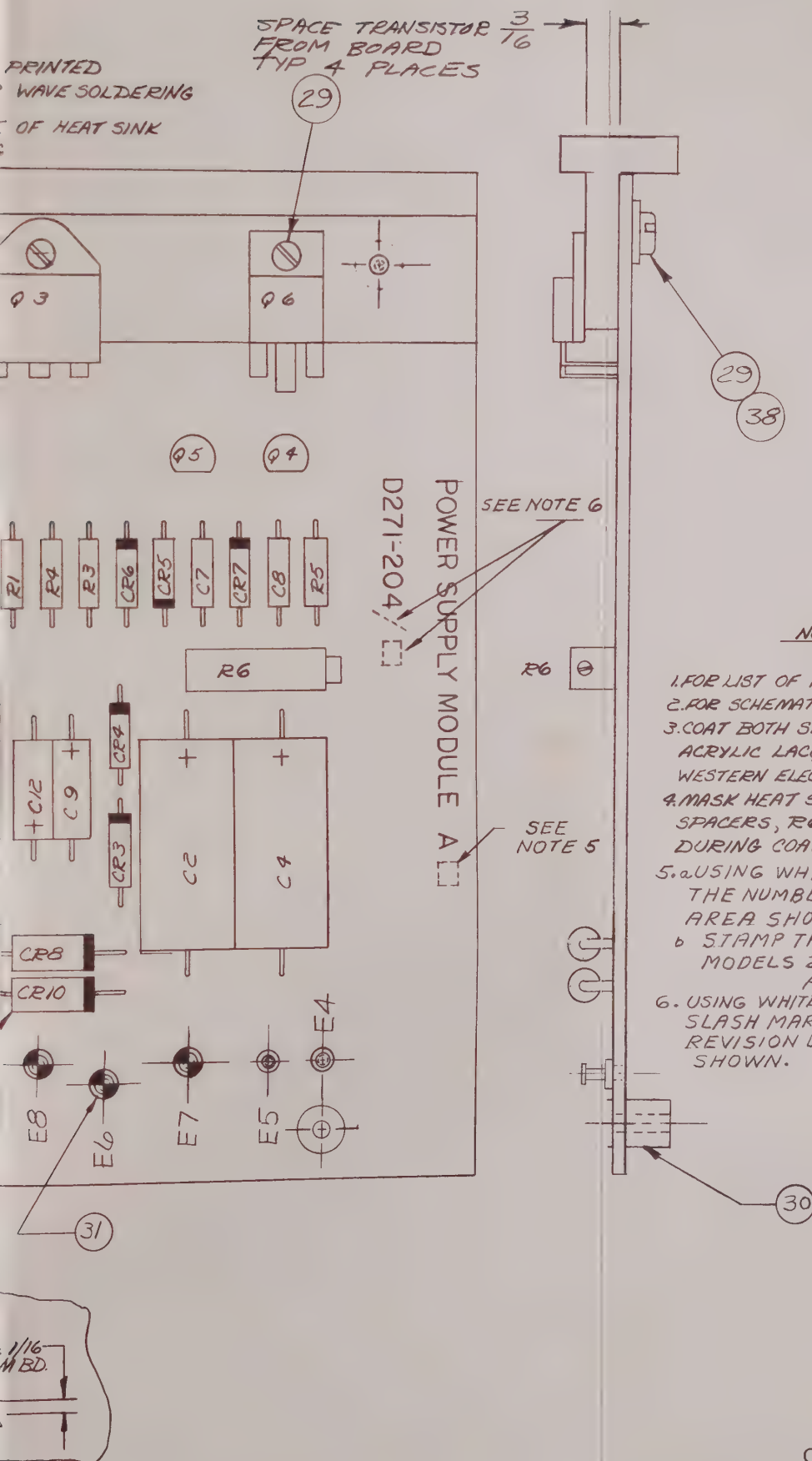
4

37

32

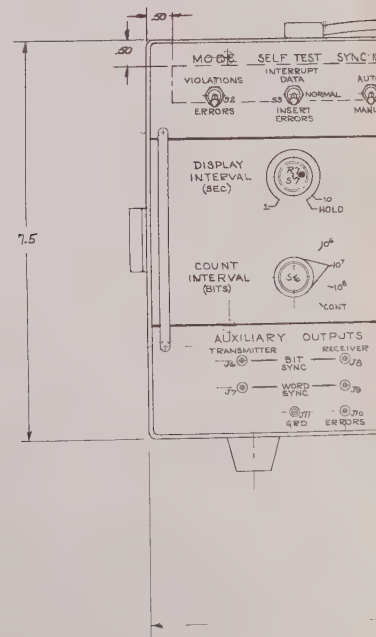
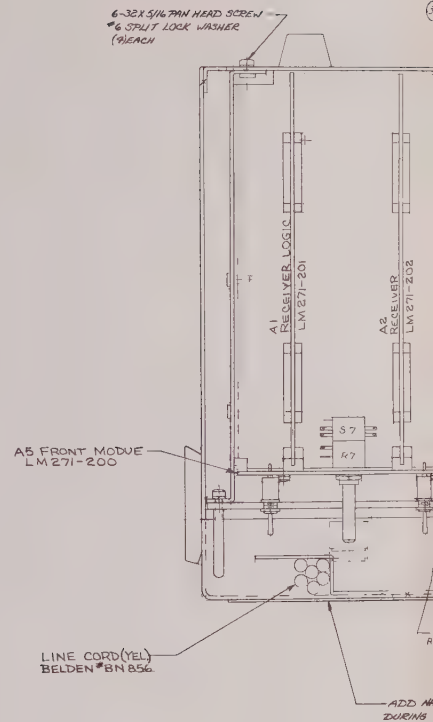
CR8 & CR10
MT
FR

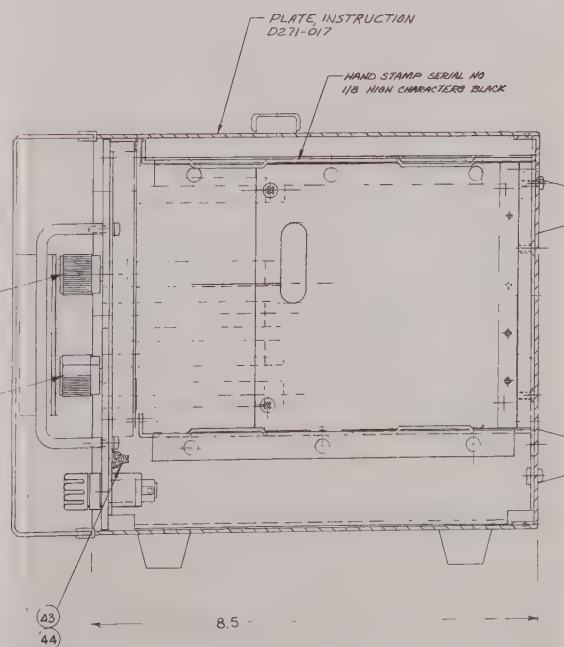
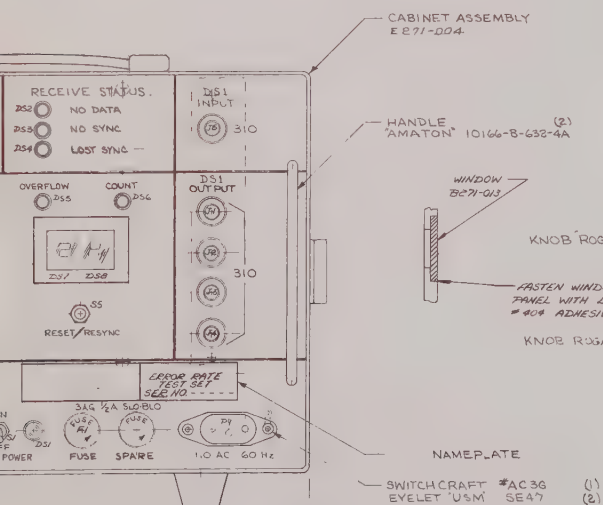
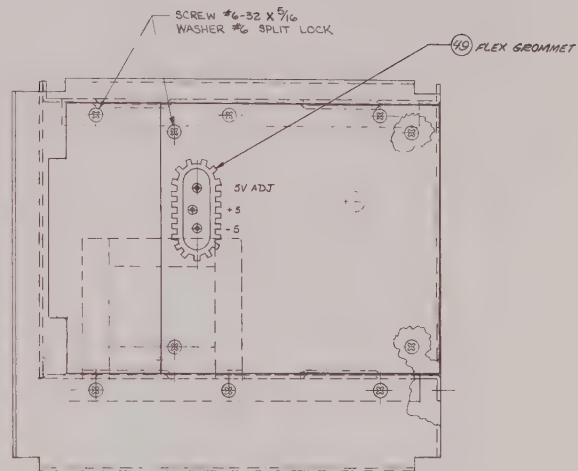
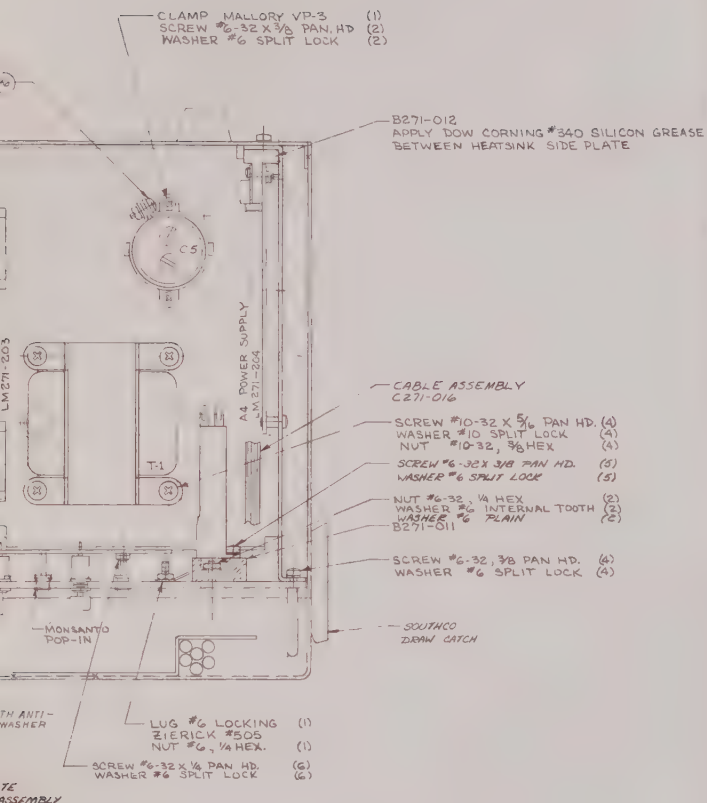


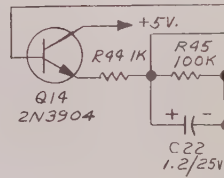
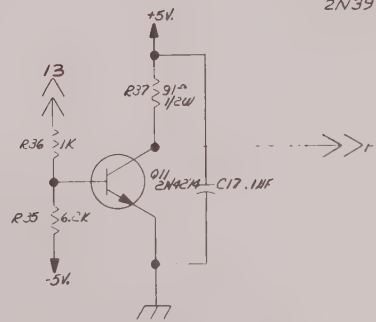
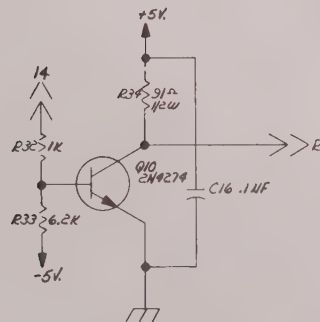
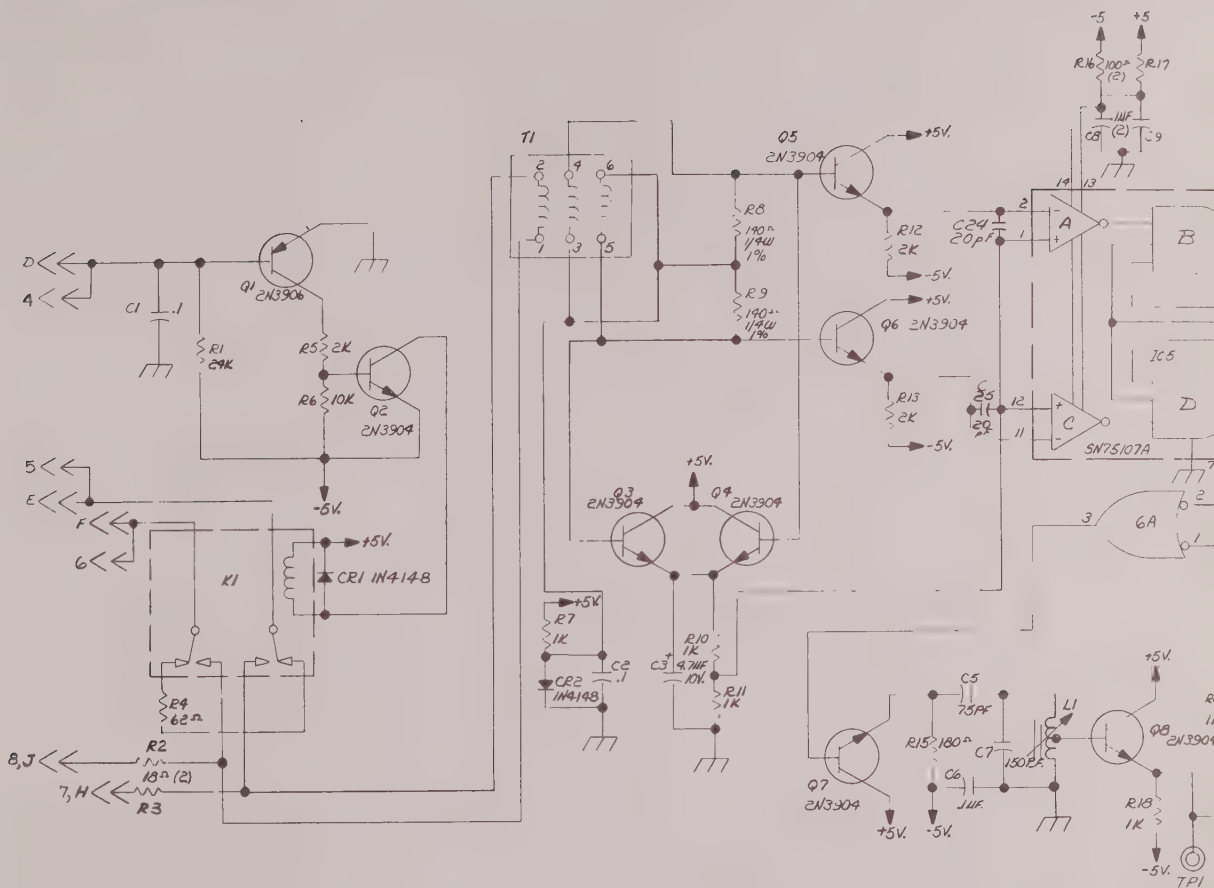


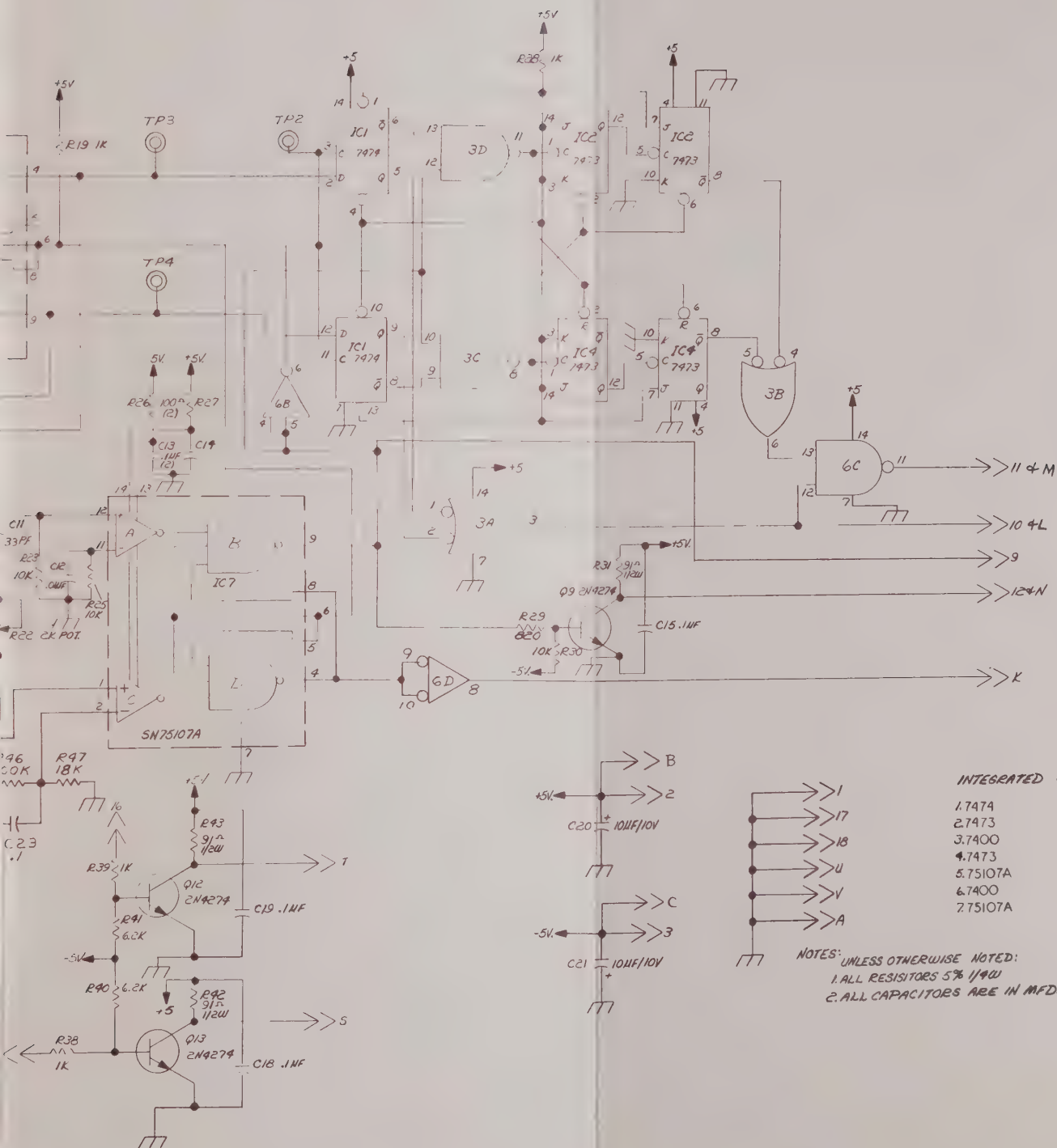
NOTES

1. FOR LIST OF MAT'L SEE LM271-204
2. FOR SCHEMATIC SEE D271-104.
3. COAT BOTH SIDES OF ASSEMBLY WITH ACRYLIC LACQUER *642 TYPE 3 PER WESTERN ELECTRIC WL-2243
4. MASK HEAT SINK AS SHOWN, (2) SPACERS, R6, & TERMINALS DURING COATING.
5. a. USING WHITE EPOXY INK, HANDSTAMP THE NUMBER 4 FOR MODEL 271A IN AREA SHOWN.
b. STAMP THE NUMBER 6 FOR MODELS 271B & 271C. IN SAME AREA.
6. USING WHITE EPOXY INK, HANDSTAMP SLASH MARK AND APPROPRIATE REVISION LETTER IN AREA SHOWN.



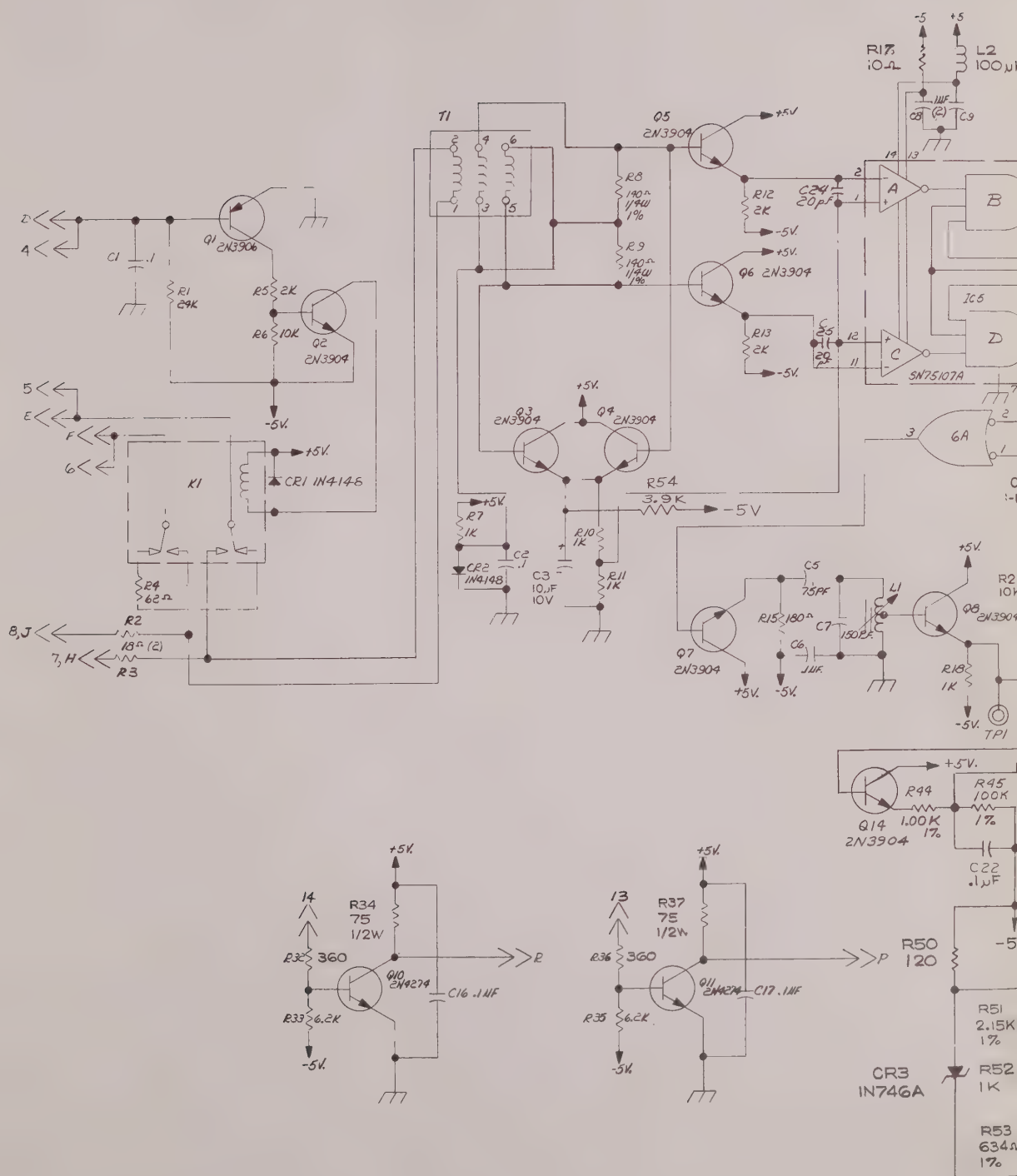


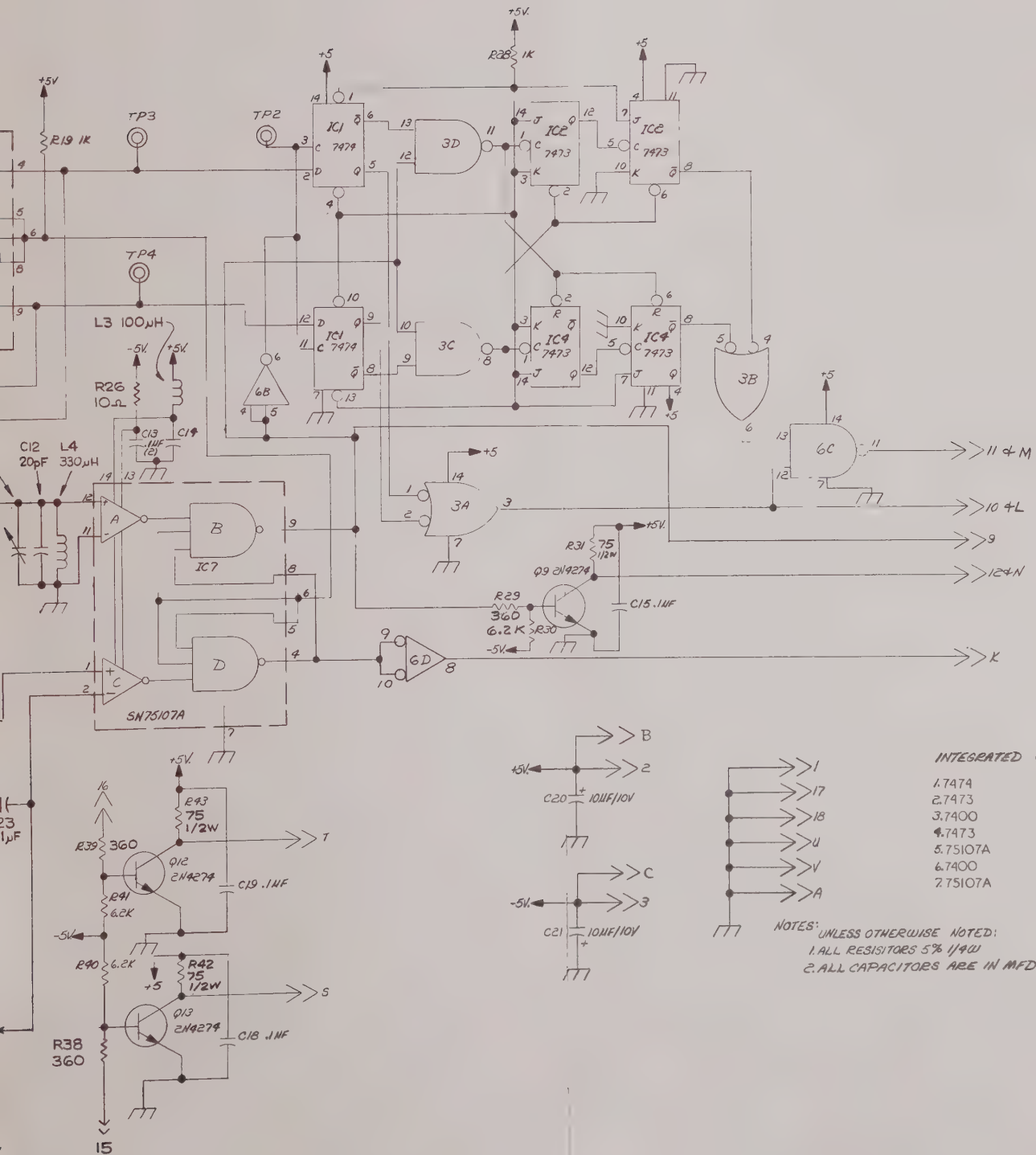




This drawing reflects an earlier revision of this printed circuit module and is included for reference purposes only.

Receiver Board Schematic
D271-102/F

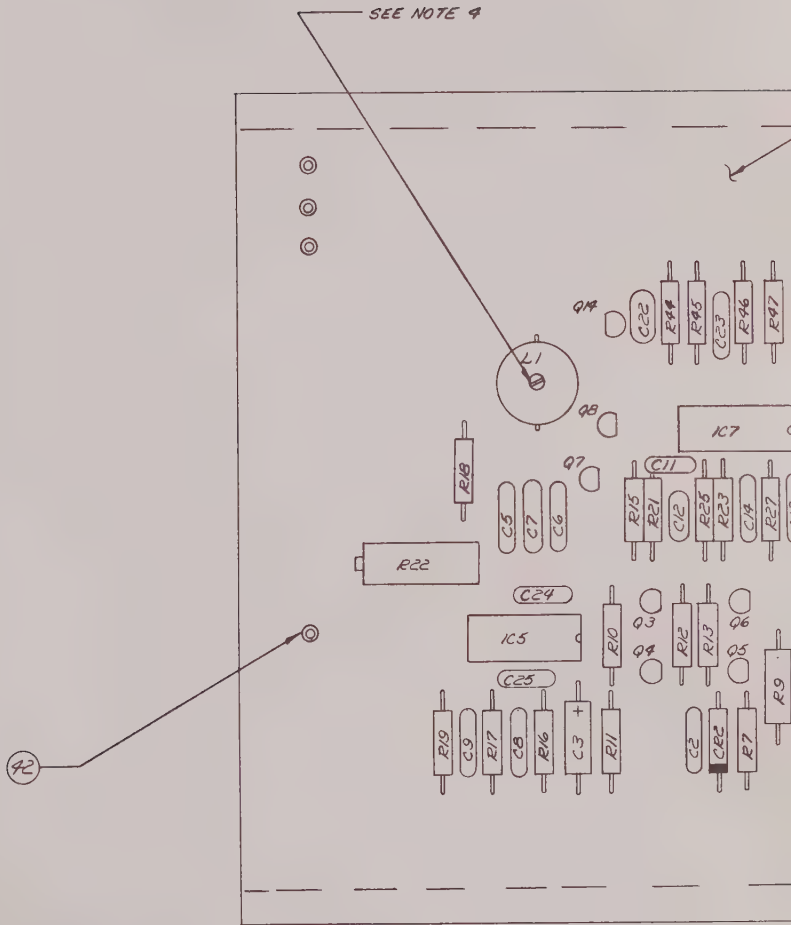


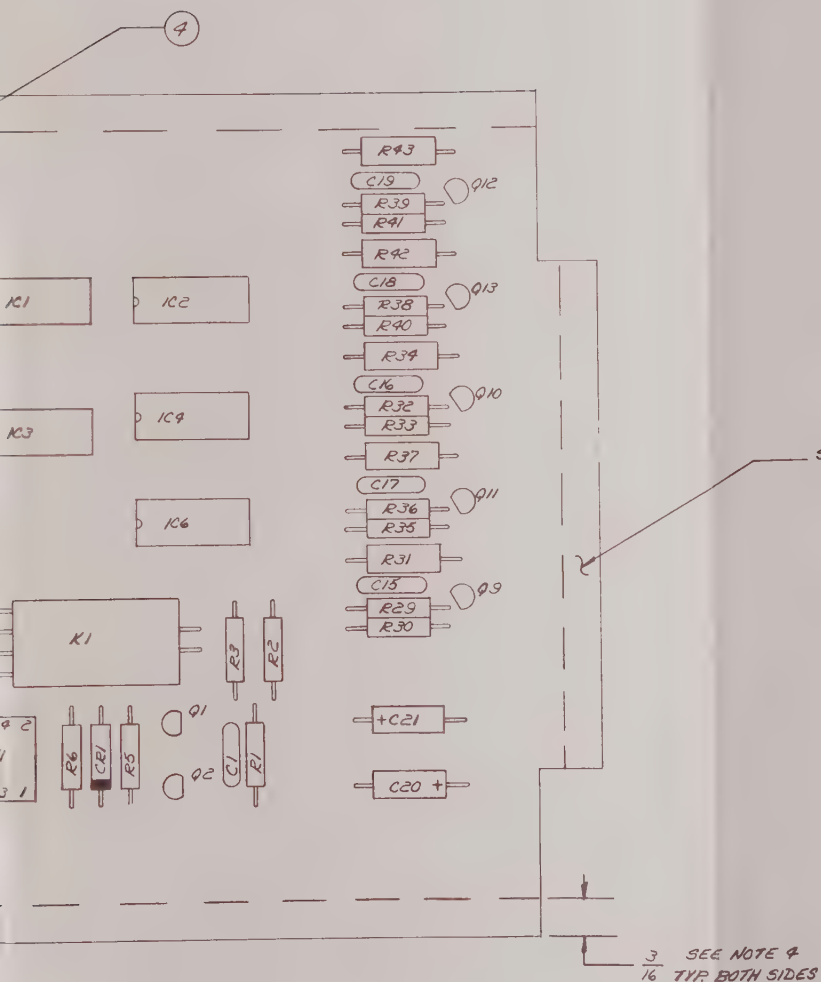


INTEGRATED CIRCUITS

1. 7474
2. 7473
3. 7400
4. 7473
5. 75107A
6. 7400
7. 75107A

NOTES: UNLESS OTHERWISE NOTED:
1. ALL RESISTORS 5% 1/4W
2. ALL CAPACITORS ARE IN MFD.'S.





NOTES

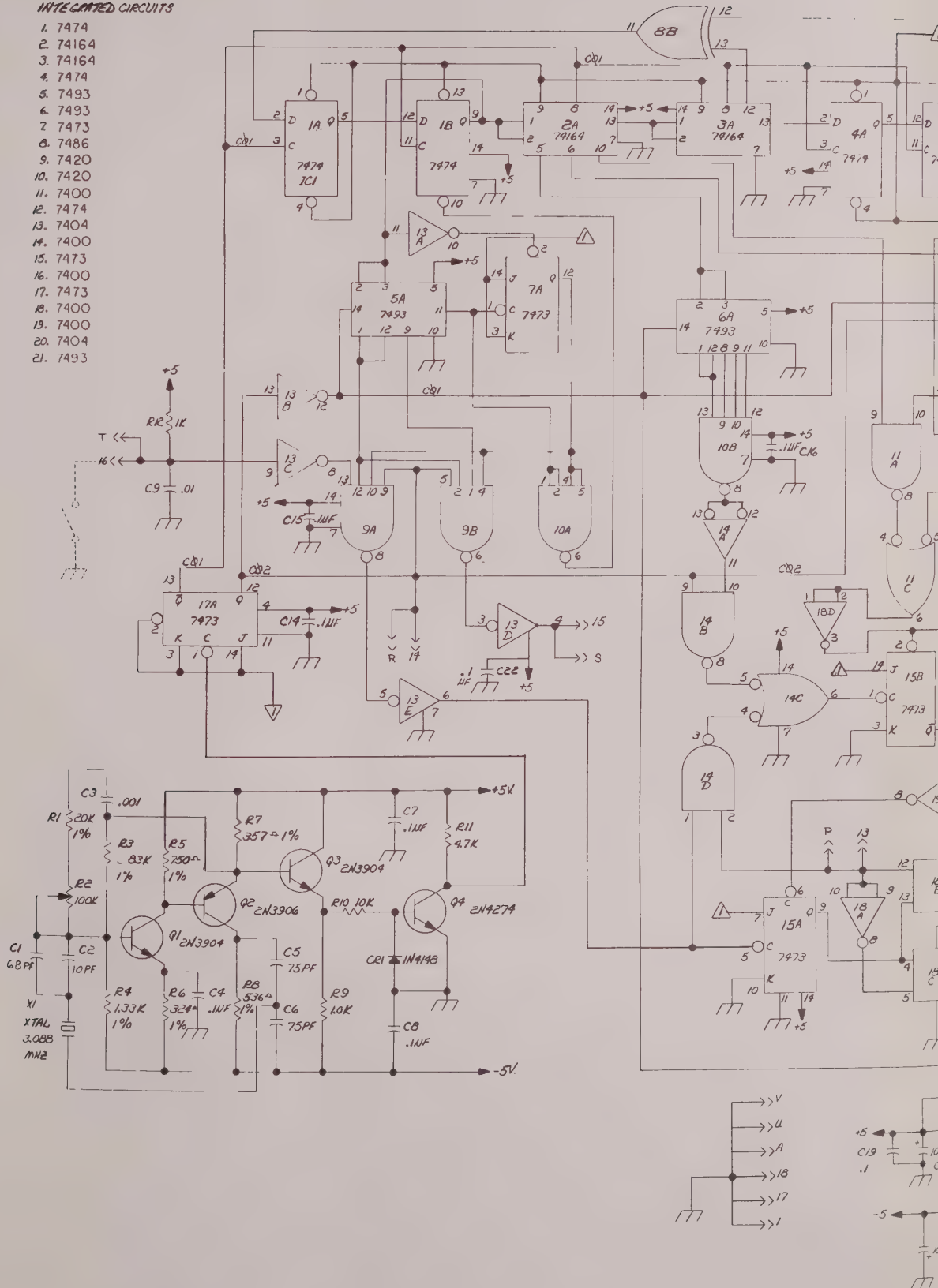
1. FOR LIST OF MAT'L'S SEE LM271-202
2. FOR SCHEMATIC SEE D271-102
3. COAT BOTH SIDES OF ASSEMBLY WITH ACRYLIC LACQUER #692 TYPE 3 PER WESTERN ELECTRIC WL-2293.
4. MASK (2) 3/16 STRIPS AND CONTACT AREA, CIRCUIT AND COMPONENT SIDES DURING COATING. ALSO MASK L1 ADJUSTMENT SCREW.

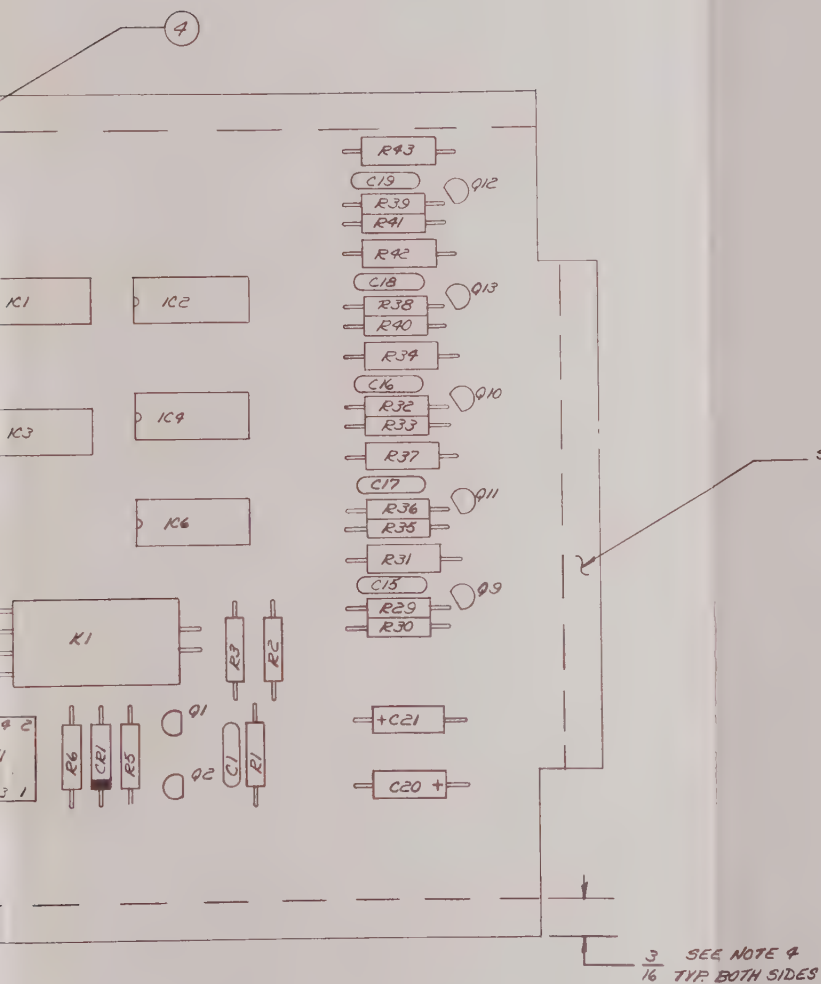
This drawing reflects an earlier revision of this printed circuit module and is included for reference purposes only.

Receiver Board Assembly
D271-202/0

INTEGRATED CIRCUITS

1. 7474
2. 74164
3. 74164
4. 7474
5. 7493
6. 7493
7. 7473
8. 7486
9. 7420
10. 7420
11. 7400
12. 7474
13. 7404
14. 7400
15. 7473
16. 7400
17. 7473
18. 7400
19. 7400
20. 7404
21. 7493

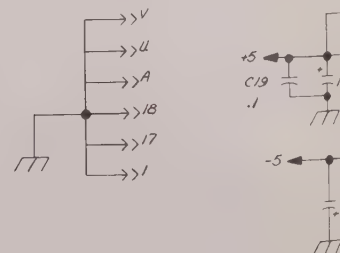
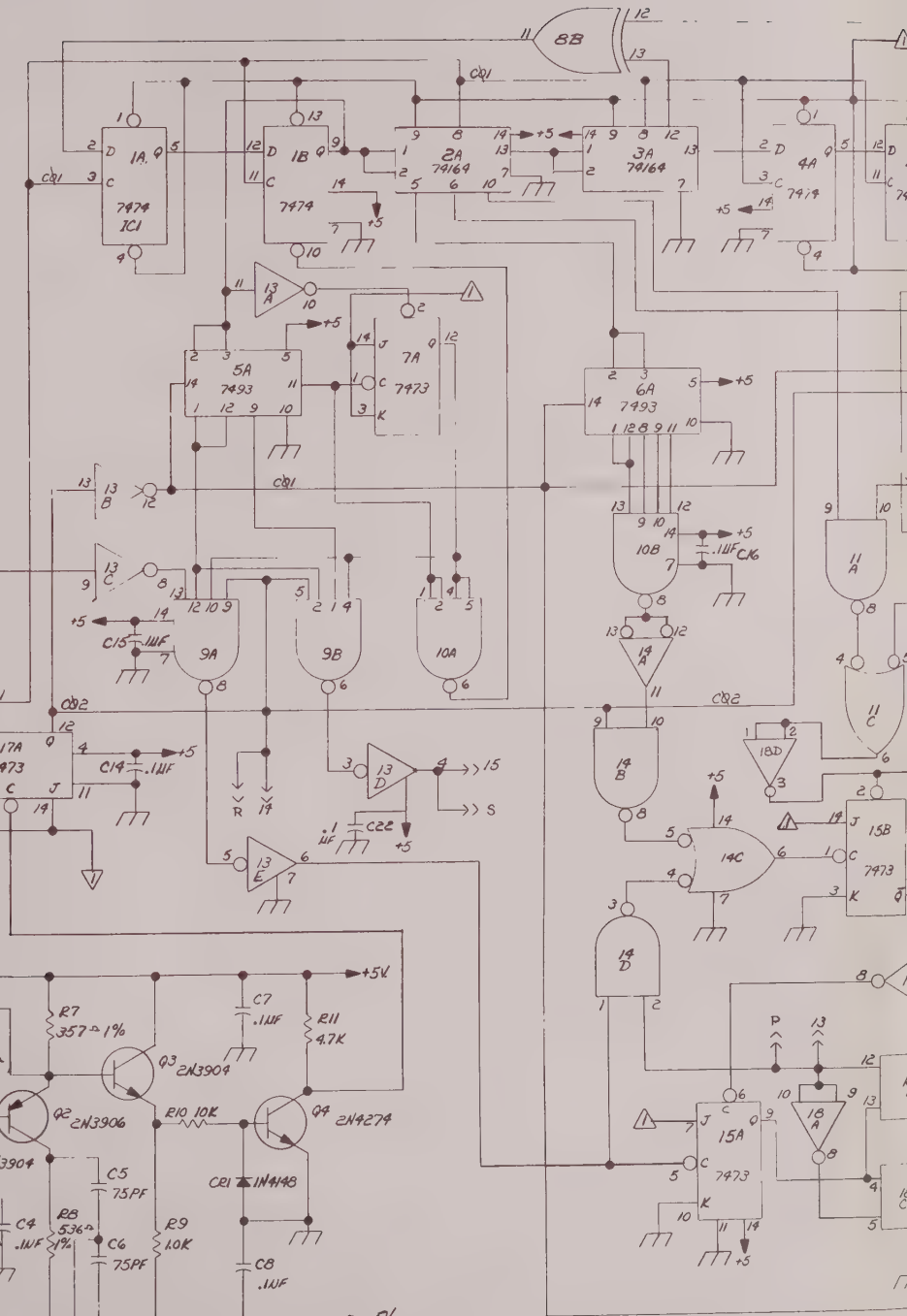
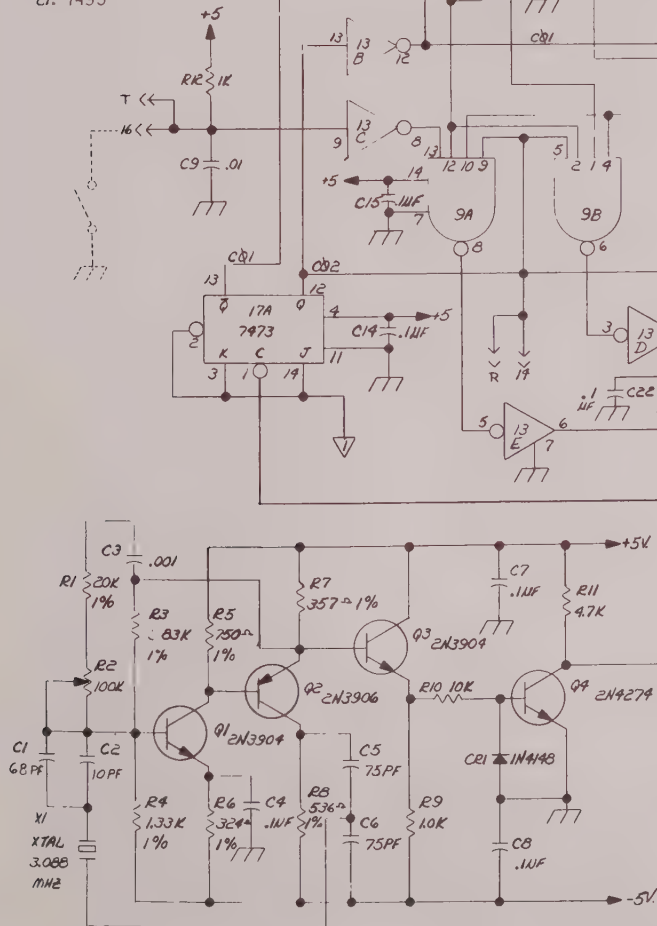


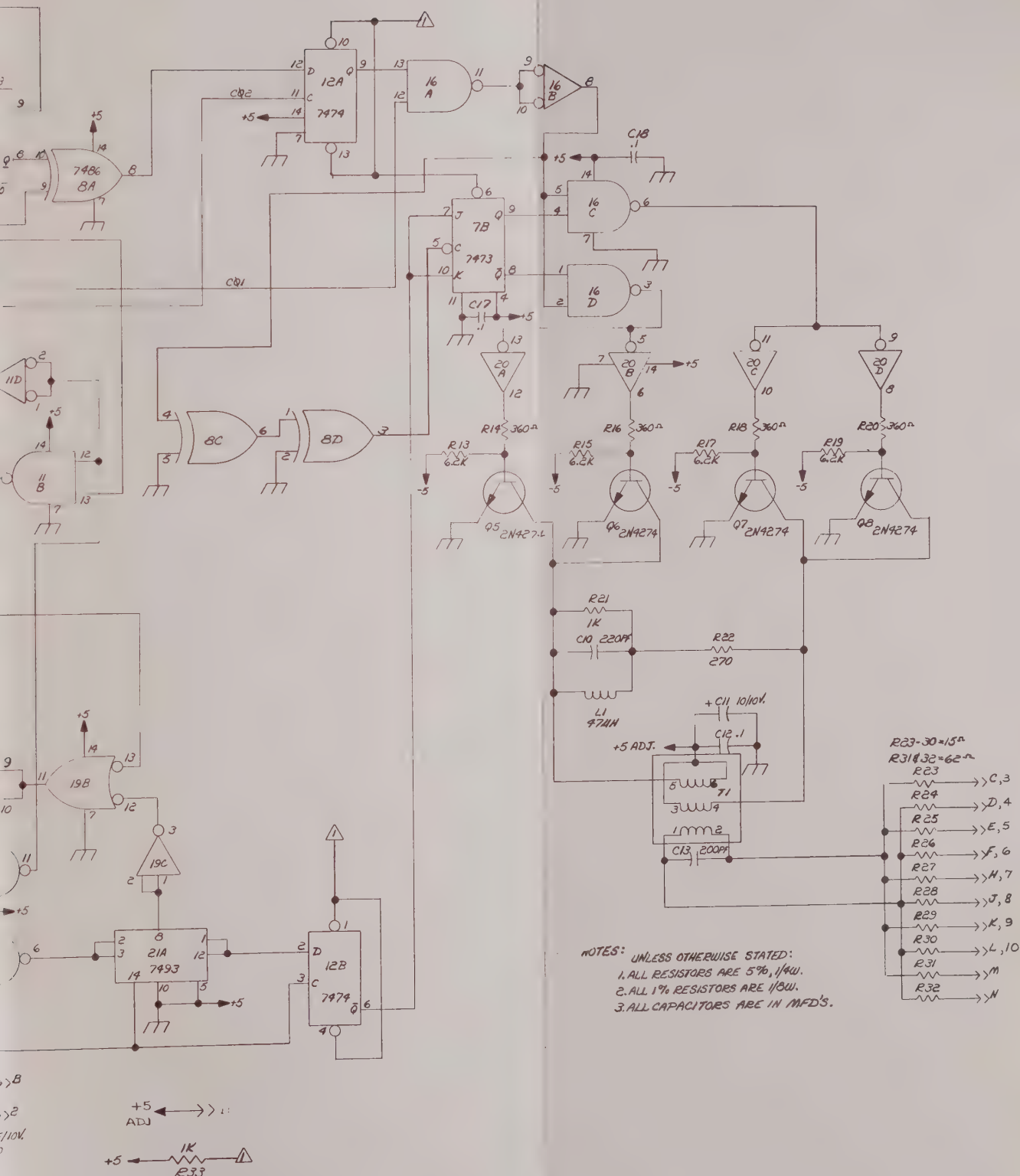


This drawing reflects an earlier revision of this printed circuit module and is included for reference purposes only.

Receiver Board Assembly
D271-202/0

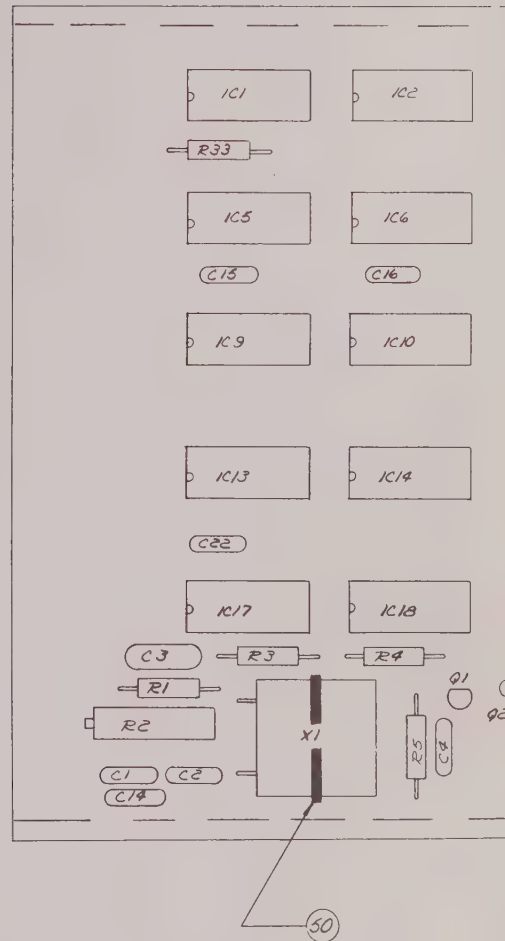
1. 7474
2. 74164
3. 74164
4. 7474
5. 7493
6. 7493
7. 7473
8. 7486
9. 7420
10. 7420
11. 7400
12. 7474
13. 7404
14. 7400
15. 7473
16. 7400
17. 7473
18. 7400
19. 7400
20. 7404
21. 7493





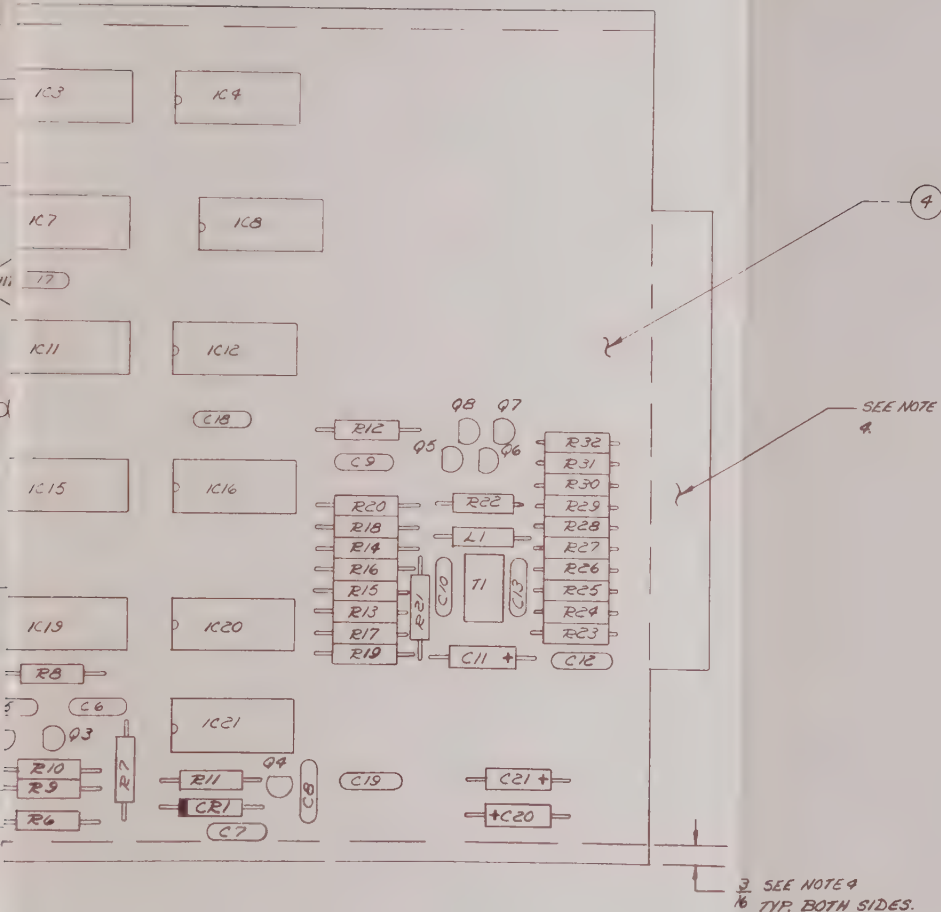
This drawing reflects an earlier revision of this printed circuit module and is included for reference purposes only.

Transmitter Board Schematic
 D271-103/C



9

9



NOTES

1. FOR LIST OF MAT'L SEE LM271-203
2. FOR SCHEMATIC SEE D271-103.
3. COAT BOTH SIDES OF ASSEMBLY WITH ACRYLIC LACQUERTM 692 TYPE 3 PER WESTERN ELECTRIC WL-2243.
4. MASK (2) 3/16 STRIPS & CONTACT AREA, CIRCUIT AND COMPONENT SIDES & R 2 DURING COATING.

SEE NOTE
A

3 SEE NOTE 4
16 TYP. BOTH SIDES.

This drawing reflects an earlier revision of this printed circuit module and is included for reference purposes only.

Transmitter Board Assembly
D271-203/0

CHAPTER 7

PARTS AND MANUFACTURERS

Items listed herein are electrical and circuit components. They are grouped under the title of associated modules. Each part is itemized by REF. DES. (Reference Designation) and described according to title, values, manufacturer, and manufacturer's identification number. Exception to providing manufacturer identification is taken where the part is standardized RETMA. Any manufacturer registered for RETMA parts will be acceptable.

A second list gives manufacturer's names, for convenience in locating specific components or related information.

<u>REF. DES.</u>	<u>COMPONENT DESCRIPTION</u>	<u>COMPONENT MANUFACTURER</u>	<u>PART NO.</u>
<u>FRONT PANEL BOARD ASSEMBLY (Schematic D271-100; Assembly D271-200)</u>			
S2, 4	Switch, SPDT	C & K	7101HCBE
S5	Switch Push Button	C & K	P8121HCE & A7527-2
S3	Switch, Momentary	C & K	7105HCBE
S6	Switch, Rotary	Oak	B6187
S7 & R7	Variable Resistor & AC Switch	A-B	B6220
IC1, 2	Int. Circuit TTL		7447A
IC3, 4	Int. Circuit TTL		7490
DS7, 8	7 Segment LED	Monsanto	MAN-1 or Equiv.
DS2, 3, 4, 5, 6	LED	Fairchild	FLV-110 or Equiv.
IC5	Int. Circuit DTL		835
R13 thru 36	Resistor, 91 Ω , 1/4W, 5%		RC07GF910J
R8 thru 12	Resistor, 150 Ω , 1/4W, 5%		RC07GF151J
<u>RECEIVER LOGIC BOARD (Schematic D271-101; Assembly D271-201)</u>			
IC8, 13, 16, 17, 21, 30	Int. Circuit TTL		7400
IC6, 12, 26	Int. Circuit TTL		7404
IC14, 19	Int. Circuit TTL		7410
IC7	Int. Circuit TTL		7420
IC10, 20, 29	Int. Circuit TTL		7473
IC1, 2, 15, 18	Int. Circuit TTL		7474
IC11	Int. Circuit TTL		7486
IC22, 23, 27, 28	Int. Circuit TTL		7490
IC5, 9, 24	Int. Circuit TTL		7493
IC3, 4	Int. Circuit TTL		74164
IC25	Int. Circuit DTL		858
Q2, 4	Transistor NPN		2N3904
Q1, 3	Transistor PNP		2N3906
CR1	Diode		1N4148
R6	Resistor, 470 Ω , 1/4W, 5%		RC07GF471J
R1, 2, 4, 5, 7, 8, 9, 10, 11, 18, 19	Resistor, 1 K, 1/4 W, 5%		RC07GF102J

RECEIVER LOGIC BOARD (Cont'd) (Schematic D271-101; Assembly D271-201)

R15	Resistor, 4.7K, 1/4W, 5%	RC07GF472J
R3, 12, 13, 16, 20	Resistor, 10K, 1/4W, 5%	RC07GF103J
R17	Resistor, 2K, 1/4W, 5%	RC07GF202J
R14	Resistor, 24K, 1/4W, 5%	RC07GF243J
C1, 2, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13	Capacitor, 0.1 μ F, Disc	UK-16-104
C14	Capacitor, 40 μ F, 10V	150D406X9010B2
C15	Capacitor, 10 μ F, 10V	TAD10TA10
C16	Capacitor, 20 μ F	C426AR/E20
C3	Capacitor, .001 μ F Disc	DD-102
		Centralab
		Sprague
		IEC
		Amperex
		Centralab

RECEIVER BOARD ASSEMBLY (Schematic D271-112; Assembly D271-212)

C1, 2, 6, 8, 9, 13, 14 15, 16, 17, 18, 19	Capacitor 0.1 μ F, 16V Disc.	Centralab	UK-16-104
C3	Capacitor 10 μ F, 10V	Sprague	150D106X9010B2
C5	Capacitor .75PF, 5% N030	Sprague	C25A102J750J
C7	Capacitor 150PF, 5% N150	Sprague	C032A102L151J
C11	Capacitor, Variable 1-18 PF	Erie	567-013
C12	Capacitor 12PF, 5%, Mica	CDE	CM04CD120J03
C20, 21	Capacitor, 10 μ F, 10V	IEC	TAD10TA10
C24, 25	Capacitor, 20PF, 5%	CDE	CD6CD200J03
C26	Capacitor 3900PF	CDE	CD19FD392J
C27	Capacitor 47 μ F, 10V	Sprague	150D476X9010B2
IC1	Int. Circuit TTL		7474
IC2, 4	Int. Circuit TTL		7473
IC3, 6	Int. Circuit TTL		7400
IC5, 7	Int. Circuit Line Receiver		75107A
IC8	NPN Transistor Array	RCA	CA3083
IC9	Int. Circuit		74123
Q1	Transistor (not MPS)		2N3906
Q2, 7, 8	Transistor (not MPS)		2N3904
Q9, 10, 11, 12, 13	Transistor NPN		2N2369A
CR1, 3	Diode		1N4148
R1	Resistor 24K, 1/4W, 5%		RC07GF243J

RECEIVER BOARD ASSEMBLY (Cont'd) (Schematic D271-112 ; Assembly D271-212)

R2, 3	Resistor 18Ω, 1/4W, 5%	RC07GF180J
R4	Resistor 16Ω, 1/4W, 5%	RC07GF620J
R5, 12, 13	Resistor 2K, 1/4W, 5%	RC07GF202J
R6, 21	Resistor 10K, 1/4W, 5%	RC07GF103J
R7	Resistor 1.6K, 1/4W, 5%	RC07GF162J
R8, 9	Resistor 140Ω, 1/4W, 1%	RN65C1400F
R10, 11, 18, 19, 58, 28	Resistor 1K, 1/4W, 5%	RC07GF102J
R15	Resistor 180Ω, 1/4W, 5%	RC07GF181J
R17, 26	Resistor 10Ω, 1/4W, 5%	RC07GF100J
R29, 32, 36, 38, 39	Resistor 360Ω, 1/4W, 5%	RC07GF361J
R30, 33, 36, 40, 41	Resistor 6.2K, 1/4W, 5%	RC07GF622J
R31, 35, 37, 42, 43	Resistor, 75Ω, 1/2W, 5%	RC20GF750J
R54	Resistor, 22K, 1/4W, 5%	RC07GF223J
R55	Resistor, 470Ω, 1/4W, 5%	RC07GF471J
R56	Resistor, 6.8K, 1/4W, 5%	RC07GF682J
R57	Resistor, 23.7K, 1/8W, 1%	RN60C2372F
T1	Transformer	PE-5762
K1	Reed Relay	UD-12-P1
L1	Tapped Inductor	B6346
L2, 3	Inductor, 100 UH	NR-100, LF-100
L4	Inductor, 330 UH	NR-330, LF-330
TP1, 2, 3, 4	Terminal Turret	2027-2
		Pulse Eng'g.
		Coto-Coil
		Aladdin Elect.
		Lenox-Fugle
		Lenox-Fugle
		Cambion

TRANSMITTER BOARD (Schematic D271-103; Assembly C271-203)

IC1, 4, 12	Int. Circuit TTL	7474
IC2, 3	Int. Circuit TTL	74164
IC5, 6, 21	Int. Circuit TTL	7493
IC7, 15, 17	Int. Circuit TTL	7473
IC8	Int. Circuit TTL	7486
IC9, 10	Int. Circuit TTL	7420
IC11, 14, 16, 18, 19	Int. Circuit TTL	7400
IC13, 20	Int. Circuit TTL	7404

TRANSMITTER BOARD (Schematic D271-103, Assembly C271-203) (Cont'd)

C3	Capacitor, 30 pF, N2200	Sprague	10TCY-Q30
C1	Capacitor, 1-18 pF	Erie	567-013
C2	Capacitor, factory select, N1500	Sprague	10TCW-Q10, Q20, Q30, Q39
C5, 6	Capacitor, 75 pF	CDE	CD6ED750J
CR1	Diode		1N4148

POWER SUPPLY BOARD (Schematic D271-104, Assembly C271-204)

CR8, 10	Diode Rectifier 3 Amp		1N4720
CR1, 2, 3, 4, 9, 11	Diode Rectifier 1 Amp		1N4003
Q1, 6	Transistor	TI	TIP-29
Q9	Transistor	TI	TIP-30
Q3	Transistor	TI	TIP-33
CR5, 7, 12	Diode		1N4148
Q2, 4, 5	Transistor NPN		2N3904
Q7, 8	Transistor PNP		2N3906
CR6, 13	Diode Zener		1N749A
R2	Resistor, 4.7K, 5%, 1/2W		RC20GF472J
R4, 9, 10	Resistor, 270, 5%, 1/2W		RC20GF271J
R3, 8	Resistor, 10Ω, 5%, 1/2W		RC20GF100
C2, 4	Capacitor, 50 μF, 50V	IEC	TAD50TK50
C1, 3	Capacitor, 25 μF, 50V	IEC	TAD25TH50
C9, 12	Capacitor, 20 μF, 16V	IEC	TAD20TC16
C8	Capacitor, .1 μF, 16V	Centralab	UK-16-104
C10	Capacitor, 470 μf, 25 V	IEC	TAD470TP25
C7, 11	Capacitor, 100 pF	CDE	CD6FC101J
C6	Capacitor, 270 pF	CDE	CD7FC271J

POWER SUPPLY BOARD (Schematic D271-104, Assembly C271-204)(Cont'd)

R1, 7	Resistor, 27K, 5%, 1/2W	RC20GF273J
R5	Resistor, 180Ω, 5%, 1/2W	RC20GF181J
R6	Pot 50Ω	89PR50
	Beckman	

MAIN ASSEMBLY (Schematic D271-100, Assembly E271-001)

J1, 2, 3, 4	Phone Jack	Switchcraft	MT-333B
J5	Phone Jack	Switchcraft	MT-336B
F1, Spare	3AG Fuse Extractor Post	Littelfuse	342014A
J11	3AF Slo-Blo Fuse 1/2A	Littelfuse	313500
J6-J10	Terminal, Gnd	Lundey	B4850
P1	Insulated, Jack	Selectro	SKT-5BC Gray
DS1	Receptacle	Switchcraft	AC3G
C5	Lamp, Glo-Dot	Industrial Devices	2150A1
	Capacitor Electrolytic 8700 μF,	GE	86F139M
	25 V dc		
T1	Transformer	Inglot	B6218
S1	Switch, SPD T	C & K	7101HQE
R1, -4	Resistor, 100Ω, 1/4W, 5%		RC07GF101J
-	Decal, Simplified Operating Instructions	Bowmar/ALI	217-017

LIST OF MANUFACTURERS

<u>Abbreviation</u>	<u>Complete Name and Address</u>
A-B	Allen-Bradley Company 1201 South Second Street Milwaukee, Wisconsin 53204 USA
Aladdin	Aladdin Electronics 701 Murfreesboro Road Nashville, Tennessee 37210 USA
Amperex	Amperex Electronics Corporation Component Division 35 Hoffman Avenue Hauppauge, New York 11787 USA
Beckman	Beckman Instruments, Inc. Helipot Division 2500 Harbor Boulevard Fullerton, California 92634 USA
Cambion	Cambridge Thermionic Corporation 445 Concord Avenue Cambridge, Massachusetts 02138 USA
C & K	C & K Components, Inc. 103 Morse Street Watertown, Massachusetts 02172 USA
CDE	Cornell-Dubilier Electronics, Inc. CDE International Marketing 2070 Maple Street Des Plaines, Illinois 60018 USA
Centralab	Centralab Electronics Division Globe-Union, Inc. 5757 North Greenbay Avenue Milwaukee, Wisconsin 53209 USA
Coto-Coil	Coto-Coil Company, Inc. 57 Pavilion Avenue Providence, Rhode Island 02905 USA
Fairchild	Fairchild Semiconductor Components Group 464 Ellis Street Mountain View, California 94040 USA

GE	General Electric Company Electronic Components Sales Department Electronics Park Syracuse, New York 13201 USA
IEC	IEC Electronics Corporation 319 East Chestnut Street East Rochester, New York 14445 USA
Industrial Devices	Industrial Devices, Inc. Edgewater, New Jersey 07020 USA
Inglot	Inglot Electronics 1145 West Diversey Parkway Chicago, Illinois 60614 USA
Lenox-Fugle	Lenox-Fugle Electronics, Inc. 100 Sylvania Place South Plainfield, New Jersey 07080 USA
Littelfuse	Littelfuse, Inc. 800 East Northwest Highway Des Plaines, Illinois 60016 USA
Lundey	Lundey/Pylon, Inc. 51 Newcomb Street Attleboro, Massachusetts 02703 USA
Monsanto	Monsanto - Electronic Special Products 10131 Bubb Road Cupertino, California 95014 USA
Oak	Oak Industries, Inc. Switch Division Department EL Crystal Lake, Illinois 60014
Pulse	Pulse Engineering, Inc. Box 12235 San Diego, California 92112 USA
Sealectro	Sealectro Corporation 225 Hoyt Street Mamaroneck, New York 10543 USA

Sprague

Sprague Electric Company
481 Marshall Street
North Adams, Massachusetts 01247 USA

Switchcraft

Switchcraft, Inc.
5555 North Elston Avenue
Chicago, Illinois 60630 USA

TI

Texas Instruments, Inc.
Components Group
Box 5012
Dallas, Texas 75222 USA

CHAPTER 8

SUPPLEMENTARY DATA

8.1 Guarantee

Bowmar/ALI, Inc. guarantees to the original purchaser that this instrument is in accordance with applicable specifications. Any deviation from these specifications and any defects in workmanship or materials will be corrected by Bowmar/ALI, Inc., provided the instrument has been properly used under normal operating conditions. This guarantee is effective for one year from date of shipment except for failure of or attributable to tubes, fuses, batteries, or semiconductors after ninety days from date of shipment. Bowmar/ALI, Inc. will be the sole judge of the validity of all claims.

All returns made under this guarantee must be authorized in writing by Bowmar/ALI, Inc. Such authorization will be given only upon receipt of information concerning type, serial number, and the defect claimed. Return shipments must be made prepaid except returns authorized within thirty days from date of shipment, in which case Railway Express Collect will be authorized. All rework done under this guarantee will be reshipped prepaid from our plant.

Bowmar/ALI, Inc. will not be responsible for, nor assume any expense or liability for, damage of loss in shipment, loss of profit, or any other damages or claims for which provisions are not specifically made herein.

8.2 Material Damaged in Shipment

Upon receipt of the instrument, do not unpack if the packing case shows evidence of damage; upon unpacking, do not discard any of the packing if damage is found which appears to have been caused

by shipment. Immediately notify the local office of the carrier and request that the damage be inspected; also, notify Bowmar/ALI, Inc. of the model number, serial number, carrier's number, date received, and any other pertinent information so that we may contact the local carrier office and facilitate a speedy settlement of any claim.

Address correspondence to: BOWMAR/ALI, INC.
531 Main Street
Acton, Massachusetts 01720 USA
Telephone: (617) 263-7756

